Design and Analysis the Performance of Ternary Logic Gates using Doping-Less FET

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***Abstract*—** This paper presents the analysis of performance and design of ternary logic gates using doping-less field-effect transistors (DLFET) integrated with resistive memory (RM). The goal which we're trying to achieve is low-power, high-speed operation suitable for multi-valued logic systems. The key ternary gates—Inverter, NAND, and NOR—are designed using DLFET-RM architecture and evaluated. Their performance is compared against conventional and emerging technologies, including Single Gate MOSFET, Double Gate MOSFET, FET, CNFET, and FINFET. Parameters such as power consumption, propagation delay, and power-delay product (PDP) are used as the basis for comparison. Significant reductions are shown for both delay and PDP in the simulation results for the proposed design. Compared to traditional logic gates, the DLFET-RM gates achieve up to 90% improvement in PDP . These improvements are hugely due to the doping-less structure, which avoids random dopant fluctuations, and the efficiency of RM elements. By eliminating the need for passive resistors, the proposed circuits also reduce area and complexity. Overall, DLFET-RM-based ternary logic is shown to be a ideal candidate for future low-power nanoelectronic systems.

***Keywords*—** *DLFET, Resistive Memory, Ternary Logic, Low Power Design, Power-Delay Product, Nanoelectronics.*

1 Introduction

Researchers have been compelled to explore non-traditional solutions for the issue of degradation and reliability concerns of complementary metal-oxide-semiconductor (CMOS) devices at the technology nodes which are small [1]. The constraints of binary logic, especially in terms of interconnect complexity, have been highlighted. [3] The interconnects occupy approximately 70% of the utilized die area, making them a significant contributor to the on-chip power dissipation. For the data intensive systems of today, the data transfer capacity of binary logic is often insufficient. Researchers have turned to multi-valued logic (MVL), which stores data at more than two levels in order to overcome these constraints.

With the potential to reduce the number of interconnects required, MVL enables increased digital transfer of data over a single wire at a given moment. [6] With this reduction in interconnect complexity and chip area, coupled with enhanced information capacity and computational efficiency, designs using MVL represents a significant advantage for digital systems . MVL can be realized using ternary (three-level) and quaternary (four-level) logic, with ternary logic being the simplest form. Ternary logic makes the pin-out challenges less severe and enhances the density of interconnects in digital systems. [4]

Ternary logic operates in two modes: unbalanced and balanced. The ternary logic which is unbalanced defines 0, 1, and 2 levels using voltages which are positive. The balanced ternary logic utilizes -1, 0, and 1 levels with positive and negative voltages [11]. The circuit designs combining both binary and ternary logic also fall under the MVL implementations. [5]

Sophisticated and intricate technologies have been developed in order to optimize power and speed in MVL systems. Using Field Effect Transistor (FET) technology, single-electron transfer technologies and quantum-dot cellular automata, MVL is implemented [6]. Among these, it is the FET technology which emerges as the most practical choice due to its support for previous generations and intrinsic similarity to CMOS structures. MVL logic requires multi-threshold devices, which DLFETs can achieve by varying their diameters.[2] The DLFETs offer superior transconductance, higher ON-to-OFF current ratios, and threshold swings which are small. Extensive research is underway to identify mechanisms and materials which are suitable with CMOS technology in order to address the challenges of expanding in nanoscale devices [10]. One promising candidate is the resistive random-access memory (RM), which exhibits expandability, non-volatility, high storage density, and elevated ON resistance at lower technology nodes. A significant interest is garnered for RM being used in

ternary logic applications though it has been predominantly utilized for binary logic [9].

This study focuses on implementing DLFET-RM-based ternary logic circuits, emphasizing reduced consumption of power, improved power-delay product (PDP), minimized area, and lower count of transistor compared to conventional implementations of ternary logic.

2 Design Methodology

2.1 Proposed Doping less FET – RM based tristate gates

The RM (resistive random access memory) is controlled by the supply of voltage across its terminals. Being as a switch, the RM replaces the Doping less FET in the design, offering the benefit of a component count reduced and minimized area overhead. The conventional CMOS resistive tristate inverter is illustrated in Figure 1. With the logic 0 applied at the input, T1 is ON and T2 is OFF, causing nil current to flow through the resistors, resulting in the output being at logic 2. When logic 2 is applied to the input, T1 is OFF and T2 is ON, driving the output to logic 0. For an input of logic 1, both transistors are ON, and the output must be logic 1, which is achieved by using larger resistor values. The proposed Doping less FET –RM based tristate inverter, shown in Figure. 2, eliminates the need for resistors by replacing them with RM, simplifying the design.

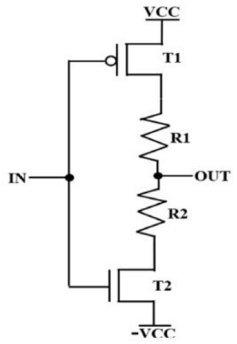

Fig. 1: Conventional CMOS resistive tristate inverter

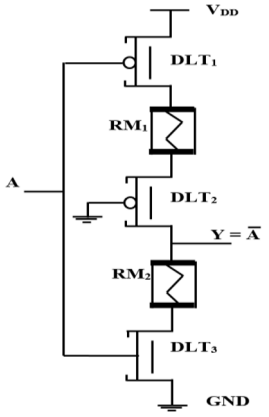

Fig 2 : Proposed Doping less FET – RM based tristate inverter

The commonly used resistive ternary inverter design employs CMOS transistors which are replaced with doping less FET (DLT1 and DLT3) and RM1 and RM2 are used instead of resistors R1 and R2, a grounded DLT2 in series with RM1 to optimize power efficiency. DLT2 is a p-channel doping less FET with its gate terminal grounded. When DLT1 is ON, the anode of RM1 is connected to VDD, causing RM1 to enter the low resistance state (LRS), which connects the source terminal of DLT2 to VDD. For DLT2, the gate-to-source voltage Vgs=Vg−Vs=0−0.9=−0.9 V, which is lower than its threshold voltage V_{th} (-0.34 V). Due to which, DLT2

Table 1 : Truth table of TNOT gate

A	DLT1	RM1	DLT2	RM2	DLT3	Y
0	Closed	LRS	Closed	HRS	Open	2
1	Closed	LRS	Closed	LRS	Closed	1
2	Open	HRS	Open	LRS	Closed	0

switches ON, creating a conductive way from the output to VDD. Conversely, when DLT1 is OFF, the anode of RM1 disconnects from the voltage which is postive, transitioning RM1 into the high resistance state (HRS). This causes the source terminal of DLT2 to reach ground potential, setting Vgs=0 V, which exceeds V_{th} .[19] Consequently, DLT2 turns OFF, functioning as a OFF device which is series connected. The combined OFF states of these two series-connected devices significantly reduce the subthreshold current, which being a major leakage power source at smaller process nodes.

In this design, DLT1 and DLT3 feature diameters of 1.30 nm, whereas DLT2 has a diameter of 1.20 nm. The RMs utilized have an oxide thickness of 11 nm, with a distance that can be between 0.1 nm and 1.5 nm, allowing for tunable resistance states. The multi-level cell capability of RMs, combined with chirality-controlled threshold voltage modulation in doping less FET, facilitates the implementation of tristate logic.

When the input is at logic 0, DLT1, DLT2 and DLT3 are in ON, ON, and OFF states, respectively. In this scenario, RM1 and RM2 are in HRS and LRS, respectively, and the output is brought to V_{DD}. For an input at logic 2, the states of DLT1and DLT3 are OFF and ON, while RM1 and RM2 transition state are LRS and HRS, respectively, pulling the output to ground (logic 0). [9]At logic 1, both DLT1 and DLT3 turn ON, with DLT2 is ON due to DLT1 ON and the voltage distribution occurs between RM1 and RM2. Since the resistances of RM1 and RM2 are equal, the voltage output drops to the half of V_{DD}. The truth table of the proposed TNOT gate under various input conditions is summarized in Table 1. The transient response and voltage transfer characteristics (VTC) of the proposed ternary inverter are depicted in Figures 3 and 4, respectively.

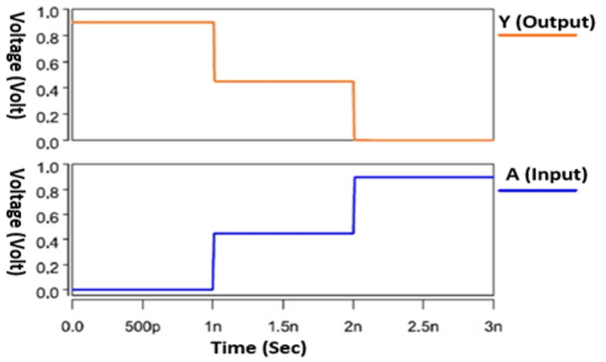

Fig. 3: Output response of the proposed ternary invertor

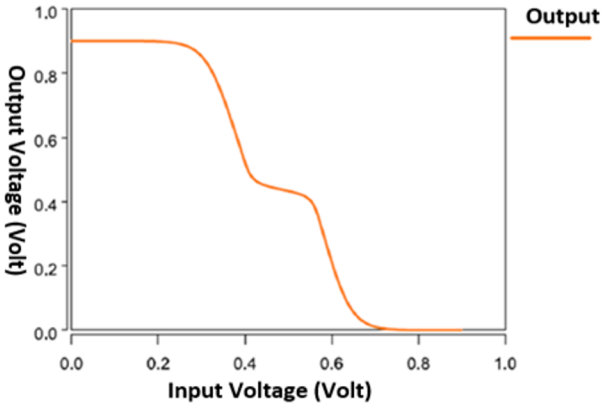

Fig. 4: Voltage transfer characteristics (VTC) of the proposed ternary inverter

2.2 Proposed T-NAND GATE

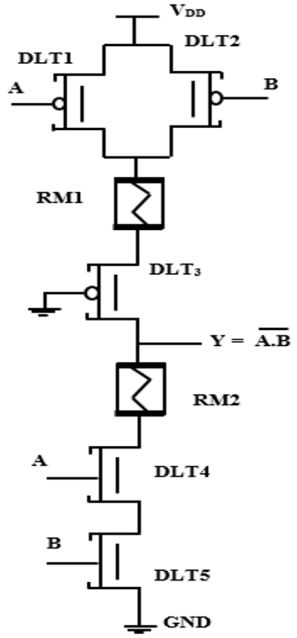

Fig 5 : Proposed Doping less T-NAND

The proposed TNAND design is showin figure 5, the chirality of Doping Less FETs DLT1, DLT2, and DLT3 is set to 17, whereas the chirality of DLT4 and DLT5 is 16. Consequently, the threshold voltage (Vth) for DLT1, DLT2, and DLT3 are -0.30 V, while for DLT4 and DLT5, it is 0.32 V. Additionally, the minimum gap distance (gap min) for the RMs used in the circuit is 1.5418 nm.

When the input to the TNAND is at logic 0, p-channel Doping less FETs DLT1and DLT2 are ON since their Vgs<Vth, while n-channel Doping less FETs DLT4 and DLT5 remain OFF due to Vgs<Vth. In this condition, the top electrode of RM1 connects to VDD, causing DLT3 to turn ON and bringing the output to logic 2.[20] For an input at logic 1, the gate-to-source voltage for p-channel Doping less FETs DLT1and DLT2 is calculated as Vgs=Vg−Vs=0.45 V−0.9 V=−0.45 V which is less than their Vth, keeping them ON. Simultaneously, for n-channel Doping less FETs DLT4 and DLT5, Vgs=Vg−Vs=0.45 V−0 V=0.45 V, exceeding their Vth, so DLT4 and DLT5 are also ON. With DLT3 ON, an equal drop of voltage occurs across RM1 and RM2, resulting in an average output voltage of 0.45 V, corresponds to logic 1. When input is at logic 2, the states of DLT1, DLT2 and DLT3 are OFF, OFF and OFF, while RM1 and RM2 transition state are HRS and LRS, respectively, DLT4 and DLT5 are ON bringing the output to ground (logic 0).

When one of the input is logic 0 and the other logic 1, the DLT1 or DLT2 is ON, and DLT3 is also ON, the output transitions to logic 2 due to either DLT4 or DLT5 is ON. When one input is logic 0 and the other is logic 2, the DLT1 or DLT2 is ON, and DLT3 is also ON, the output transitions to logic logic 2 due to either DLT4 or DLT5 is ON .[16] When one input is logic 1 and the other is logic 2, the DLT1 oR DLT2 is ON, and DLT3 is also ON, the output transitions to logic 1 due to either DLT4 and DLT5 are ON. The detailed operation of the proposed TNAND gate under various input conditions is summarized in Table 2.

Table 2 : Truth table of proposed T-NAND gate

Input		Device state							Output
A	B	DLT1	DLT2	RM1	DLT3	RM2	DLT4	DLT5	Y
0	0	Closed	Closed	LRS	Closed	HRS	Open	Open	2
0	1	Closed	Closed	LRS	Closed	HRS	Open	Closed	2
0	2	Closed	Open	LRS	Closed	HRS	Open	Closed	2
1	0	Closed	Closed	LRS	Closed	HRS	Closed	Open	2
1	1	Closed	Closed	LRS	Closed	LRS	Closed	Closed	1
1	2	Closed	Open	LRS	Closed	LRS	Closed	Closed	1
2	0	Open	Closed	LRS	Closed	HRS	Closed	Open	2
2	1	Open	Closed	LRS	Closed	LRS	Closed	Closed	1
2	2	Open	Open	HRS	Open	LRS	Closed	Closed	0

2.3 Proposed T-NOR GATE

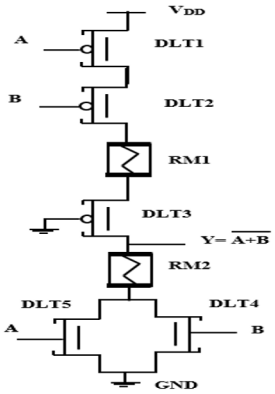

Fig 6 : Proposed Doping less T-NOR

In the designed TNOR circuit which is shown in figure 6, the V_{th} of p-channel DLT1 and DLT2 is -0.28 V, while the Vth of n-channel DLT4 and DLT5 is maintained at 0.28 V by modifying their chirality to 20, whereas the DLT3 charality is set to 18, which results in a Vth of -0.31 V.[12] Additionally, the RMs incorporated in the TNOR design have a gap min of 1.790 nm. If both inputs are logic 2, then both the DLT1 and DLT2 are OFF, while DLT4 and DLT5 are ON. As both the DLT1 and DLT2 are OFF, the RM1's top electrode is disconnected from VDD and the output is pulled to logic 0 via RM2, DLT4 and DLT5. When one input is logic 0 and the other is logic 1, both DLT1 and DLT2 are activated, turning ON the DLT3, while DLT4 or DLT5 are turn ON, leads to an equal voltage drop across the two RMs and driving the output node to logic 1. If both inputs are at logic 0, then both DLT1 and DLT2 are ON, while DLT4 and DLT5 are OFF. RM1 and RM2 enter into HRS and LRS respectively and the output is brought to logic 2. When one input is logic 0 and the other is logic 2, either DLT1 or DLT2 are OFF, the top electrode of RM1 is removed from VDD and the output is pulled to logic 0 via RM2 and DLT4 or DLT5. When one of input is logic 1 and the other logic 2, either DLT1 or DLT2 are ON, RM1 enter into HRS, DLT4 and DLT5 are ON, the output is brought to logic 0 via RM2, DLT4 and DLT5. The truth table for the TNOR proposed is presented in Table 3. The transient waveforms of DLFET-RM-based TNAND and TNOR circuits are presented in Fig. 7.

Table 3 : Truth table of proposed T-NOR gate

A	B	DLT1	DLT2	RM1	DLT3	RM2	DLT4	DLT5	Y
0	0	Closed	Closed	LRS	Closed	HRS	Open	Open	2
0	1	Closed	Closed	LRS	Closed	LRS	Open	Closed	1
0	2	Closed	Open	HRS	Closed	LRS	Open	Closed	0
1	0	Closed	Closed	LRS	Closed	LRS	Closed	Open	1
1	1	Closed	Closed	LRS	Closed	LRS	Closed	Closed	1
1	2	Closed	Open	HRS	Closed	LRS	Closed	Closed	0
2	0	Open	Closed	HRS	Closed	LRS	Closed	Open	0
2	1	Open	Closed	HRS	Closed	LRS	Closed	Closed	0
2	2	Open	Open	HRS	Open	LRS	Closed	Closed	0

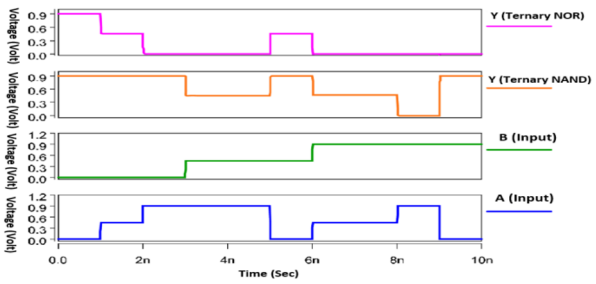

Fig. 7: Output response of the proposed T-NOR & T-NAND

3 Result and Discussion

It analyzes performance of doping-less FETs integrated with resistive memory based ternary logic gates by comparing them with popular technologies such as Single Gate MOSFET, Double Gate MOSFET, FET, CNFET, and FINFET. In the analysis of crucial parameters—power consumption, delay, and power-delay product (PDP)—under realistic operation for the performance of the proposed design, all gates tested gave DLFET-RM methodology an edge in not only improving efficiency but also simplicity through the elimination of doping as well as component reduction. It presents an efficient and power-aware solution for multi-valued logic circuits.

3.1 Ternary Inverter

Considering the ternary inverter first, the designed ternary inverter provides 0.923 ps of delay and 38.17 pW of consumption, thus providing a PDP of only 35.23 zJ. In comparison, the inverter designed using Single Gate MOSFET exhibits 3.295 ps of delay and 293.38 zJ of PDP. It corresponds to almost an 88% reduction in the PDP, translating into a tremendous saving in energy. Although the Double Gate MOSFET inverter comes slightly closer at 123.46 zJ—approximately 2.5× the proposed invertor design, the comparison among the rest of the advanced technologies for FET-based invertor results in 387.74 zJ of PDP, and 252.33 zJ as well as 89.87 zJ for CNFETs as well as FINFETs respectively as shown in figure 8. Even the finest among the available technologies, FINFET, ends up using more than 60% more energy compared to the DLFET-RM invertor. These savings are primarily due to the lack of random dopant fluctuations in DLFETs as well as the efficient switching characteristic facilitated by the use of RM in replacing passive resistors as well as facilitating an optimization of the voltage division for ternary states.

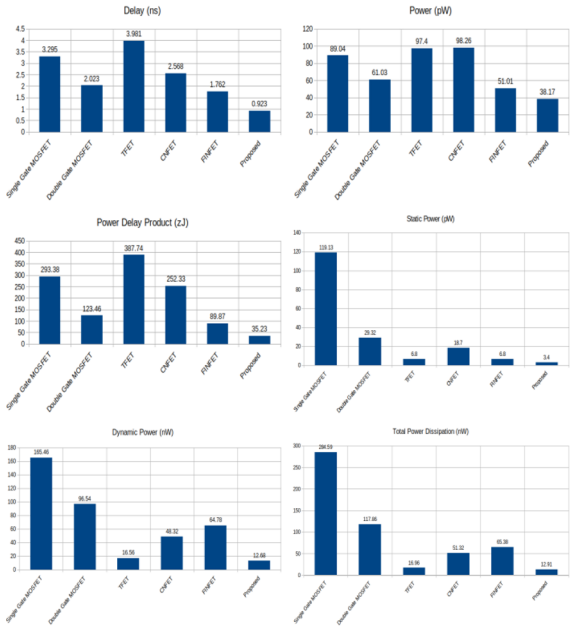

Fig. 8: Analysis of the proposed Ternary Invertor

3.2 Ternary NAND

Superior performance trend persists in the ternary NAND gate. The DLFET-RM-based NAND proposed has 2.382 ns as the delay value and 108.52 pW as the power consumption resulting in 258.49 zJ as the PDP. Comparing the DLFET-RM-based NAND when the

Single Gate MOSFET NAND reaches 2913.30 zJ as the PDP value, the DLFET-RM-based NAND demonstrates an improvement of almost 91%. In comparison, the Double Gate MOSFET NAND reaches 3434.47 zJ as the PDP value—over 13 times larger compared to our outcome. FET-based NAND circuits using 1750.58 zJ as the PDP value run at 1750.58 zJ, the CNFETs at 2480.43 zJ, as well as FINFETs at 662.01 zJ. Even when compared with the best optimized of the rest, the DLFET-RM configuration exhibits an improvement of more than 60% for the PDP as shown in figure 9. It is due to the use of doping-less FETs featuring tunable diameters so as to regulate the threshold voltages almost exactly and greatly decrease the leakage power. In addition, the use of the components for the RM aids in the restriction of the current supply during logic transition resulting in the small power profile without losing speed.

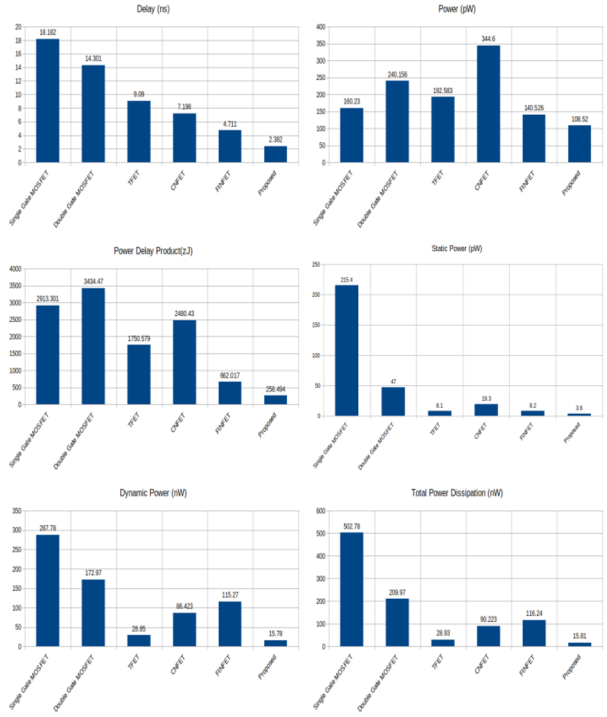

Fig. 9: Analysis of the proposed T-NAND

3.3 Ternary NOR

Promising performance is achieved for the ternary NOR gate, for which the suggested circuit realizes a delay of 2.496 ns, power of 108.99 pW, and a PDP of 272.04 zJ. In comparison, the Single Gate MOSFET version accomplishes 3923.81 zJ of PDP, whereas the Double Gate version surpasses it with 4188.93 zJ as shown in figure 10. It translates into the reduction of the PDP by well over 93% in both the cases. FET and CNFET NOR gates also lag behind, accompanying the PDPs of 2589.38 zJ and 3461.25 zJ respectively. Even FINFET-based NOR circuits accomplishing the relatively lower value of 957.65 zJ of PDP still suck up almost 71% more energy as compared to the DLFET-RM-based proposed circuit. It may all be due to the low value of the subthreshold swing of DLFETs and the control of the resistance states offered by RM so as to allow for exact values of voltages for ternary logic without superfluous static consumption of power. RM being capable of effortlessly changing between the resistance states nullifies the need for the use of the complex resistor networks so simplifies the circuit but at the same time boosts the reliability of the circuit.

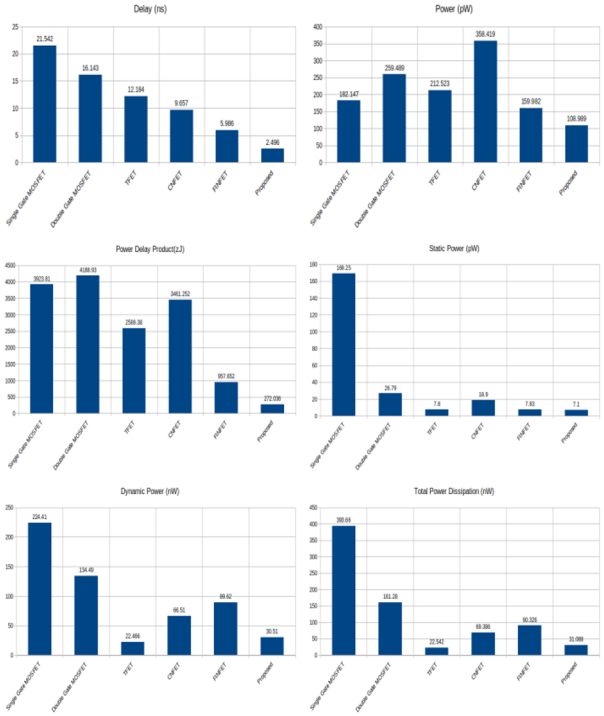

Fig. 10: Analysis of the proposed T-NOR

In combination, the findings unequivocally show DLFET-RM-associated ternary gates dominating all the rest of competing technologies on the main performance parameters. Removing doping altogether and employing charge plasma for carrier invocation not only enables the design to circumvent the variability problem characteristic of conventional MOSFETs but also reduces fabrication complexity. The RM components also lend their assistance by providing programmable resistance values useful for ternary logic voltage-level control as well as leakage reduction. Due to their small-size structure, fewer device count, as well as minimized thermal budget, DLFET-RM circuits as a whole stand out which makes them not only more energy efficient but also more scalable for contemporary VLSI applications.
To summarize , the DLFET-RM configuration reduces the delay and energy consumption up to 60-90% improvement in the PDP for different types of gates as well as different comparator technologies. All these factors certainly makes DLFET-RM an extremely efficient base platform for deploying effective multi-valued logic gates for the forthcoming nanoscale computing landscapes.

4 Conclusion

This study presents the ternary logic gates design using doping-less FETs combined with resistive memory (RM), with the aim to improve energy efficiency and reduce complexity. The DLFET structure avoids random

dopant fluctuation and enhances threshold voltage control by eliminating doping through charge plasma techniques. Resistive memory replaces traditional resistors, simplifying design and reducing circuit area and component count. The proposed ternary inverter achieves a delay of just 0.923 ns and a PDP of 35.23 zJ, significantly outperforming conventional MOSFET-based designs. In the case of the ternary NAND gate, the proposed circuit shows a PDP of 258.49 zJ, compared to over 2900 zJ in Single Gate MOSFET-based implementations—a **reduction of nearly 91%**. The ternary NOR gate follows a similar trend, with a PDP of 272.04 zJ, improving by more than **70%** compared to FINFET and over **90%** compared to traditional MOSFETs. Overall, the proposed gates reduce delay by up to 85% and power consumption which is lower across all logic types. Compared to FET, CNFET, and FINFET technologies, DLFET-RM circuits consistently deliver better PDP and reduced static power. Their compact structure, reduced thermal budget, and low leakage make them ideal for next-generation multi-valued logic systems. In conclusion, DLFET-RM based ternary gates provide a scalable, energy-efficient alternative for future nanoscale computing architectures.

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