A Coarse-Fine Time-to-Digital Converter

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Abstract. A design of time-to-digital converter (TDC) using a coarse-fine conversion scheme is presented. The coarse stage was accomplished by a delay line, and used a loop counter at the end of the delay line to achieve wide dynamic range. The fine stage utilized the dual DLL structure to achieve high precision. The proposed TDC can provide high resolution with less chip area. With an input reference clock of 125MHZ, the TDC achieves 8ps resolution, and the dynamic range achieves 1.5 μ s.

1 Introduction

Time to digital converter(TDC) is used to measure a short time interval, convert the time signal into a digital signal. With the rapid development of CMOS technology, time digitization had been widely used in physics, military and medicine science such as identify the particles by measuring their life time, in some high energy experiment, detect the distance between two target items by measuring the time interval between emission and reflection signals in laser range finder, rebuild the coordinate information of an annihilation event by measuring the particle's time of flight(TOF) in positron emission tomography(PET). Besides, TDC also plays an important role in logic analyzer, oscilloscope, etc[1].

There are two methods to design a TDC, analog approaches and digital approaches. Traditional analog approaches use time amplifier(TA)[2] or time to voltage converter(TVC) [3]to achieve high resolution, but these methods are area-consuming and with, higher cost, lower conversion rate and higher power supply comparing with digital approaches. As for digital TDC, high resolution is achieved by using the gate delay of the delay cell as TDC's quantization step. Several structures have been proposed before: The traditional structure is the single stage linear delay line, it can achieve wide range by sacrificing chip area. the Phase Locked Loop(PLL) and Delay Locked Loop(DLL) are also typically used, due to the difference of their configuration, DLL is preferred for its stability and fast locking time. Another structure named Vernier Delay Line(VDL), it provides excellent resolution but also suffer from large chip area if wide range is required.

Field-programmable gate array(FPGA) based TDC and application specific integrated circuit(ASIC) based TDC are the main technical ways to design a time to digital converter. Even the former take less time, it can hardly achieve high precision, while the ASIC based TDC has a better performance.

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Recent years' research results are as follows: Richard C's team from the University of Florida proposed a novel Vernier ring TDC in 2010, this kind of TDC places the Vernier delay cells and arbiters in a ring format and reuses them for the measurement of the input time interval, finally it can achieve a large detectable range of 12 bits with a resolution of 8ps. In 2012, Professor Luca Vercesi's team from Italy improved Vernier TDC by using two dimensions Vernier line instead of the single dimension one, this new structure help Vernier TDC achieve wide range with on area sacrifice. It comes out with the resolution of 17.2ps and dynamic range of 160ns. After that, researchers from A&M university use the loop counter both in coarse quantization and fine quantization to get wide dynamic range, and the TDC realized with a time resolution of 8.12ps and wide dynamic range of 204.8ns.

Even though the researches above tried different structures to improve TDC's resolution, the cost of chip area and power supply are also very important, so how to optimize a TDC without the sacrifice of the factors above is still a research highlight. The TDC presented in this paper aims at achieving higher precision, wide range and small chip area. The paper is structured as follows: the principle of TDC is described in Section II. The architecture of the proposed TDC is presented in Section III. Section IV presented the circuit structure, the simulation and conclusions are drawn in Section V.

2 Principle of operation

Time to digital converters usually accept two asynchronous input signals: START and STOP, measure the time interval between these two signals can convert continuous time signal into discrete digital signal. A traditional method to measure the time interval is shown in Figure.1[4].

Figure 1. Timing diagram of conversion

The measured time interval consists of three parts: the time interval Δt_1 between START signal and the succeeding rising edge of the reference clock, the time interval Δt_2 between STOP signal and the succeeding rising edge of the reference clock, and the time interval Δt_{12} between the two rising edges mentioned above. Then, the time interval Δt between START and STOP can be determined as $\Delta t = \Delta t_1 + \Delta t_{12} - \Delta t_2$. In this architecture, TDC can get wide dynamic range but its resolution is limited by the frequency of the reference clock, so this kind of TDC usually used as the coarse measure stage.

Another typical architecture of TDC is based on delay line shown in Figure.2. The delay line consists of a set of tapped delay cells and D-flip/flops(DFF), and the delay time of every tapped delay cell is set to be τ , so that τ is the quantization step. When TDC works, the INPUT signal broadcast through the delay line, DFF start to sample the status of the delay line when STOP signal comes, the time interval can be calculated by counting the number of delay cell the START signal has passed. The sampling results of the DFFs are $P_0 \sim P_{n-1}$. Delay line can achieve gate resolution, but it may cost a lot of delay cells to match the wide range required. Besides, traditional delay line is suffered from error accumulation, with the addition of the delay cell, the delay time of delay cell becomes instable and the error will increase.

Figure 2. Architecture of tapped delay line

DLL is widely used in TDC in order to improve the precision. The block diagram of the conventional analog DLL is shown in Figure.3. DLL consists of four parts: a Phase Detector(PD) which sometimes be replaced by a Phase Frequency Detector(PFD), a Charge Pump(CP), a Loop Filter(LP) and the Voltage Control Delay Line(VCDL). In the DLL, the reference clock, CLK_IN, is propagated through the voltage control delay line. A PFD is used to compare CLK_IN with the output signal, CLK_OUT, at the end of the delay line. If PFD detect a phase difference between CLK_IN and CLK_OUT, the closed loop system will automatically correct it by changing the control voltage through the charge pump, which can finally change the delay time of the VCDL. However, if the initial delay time of the VCDL is shorter than $0.5T_{clk}$ or longer than $1.5T_{clk}$, the DLL may fail to lock or falsely lock to two or more periods. That means the DLL must lock the delay time to one clock cycle of the reference signal, the initial delay time of VCDL must between $0.5T_{clk}$ and $1.5T_{clk}$. DLL based TDC can achieve the resolution of CLK_IN/n , n is the number of delay cell in VCDL.

Figure 3. Block diagram of DLL

3 Architecture design

Considered both precision and dynamic range, the Coarse-Fine TDC we proposed in this paper including three stages as shown in Figure.4. At the first level, the time interval between the rising edge of the START and STOP signal is digitized by a looped delay line. The looped delay line comprises a set of delay cell and a digital 6 bits counter at the end of the delay line. The resolution of the first stage is set to be τ_{coarse} , which is the delay time of every delay cell in this stage. The looped architecture can effectively enhance the dynamic range of the whole TDC. Then the remained time interval which is shorter than τ_{coarse} are sent into the middle stage. In order to improve the convert efficiency and led to a small chip area, we add a middle stage with a resolution of τ_{middle} . The third stage use a dual-DLL based VDL to achieve high precision, two control voltage generated from dual-DLL controls fast delay line and slow delay line of VDL respectively, and the resolution is determined as T_{CLK}/n^2 .

Figure 4. Proposed TDC architecture

3.1 A looped delay line

Conventionally, a delay line and a set of DFFs are needed in a phase sampler as Figure.2, a digital counter is added at the end of delay line to achieve wide range as shown in Figure.5[5]. When coarse quantization stage works, the rising edge of the START signal propagates through the delay line, the loop time of the START signal is stored in the counter. When the STOP signal comes, the propagate status are sampled to the DFFs and the digital counter stop to work. The time interval measured by the coarse stage can be determined as:

$$B = B_{coarse} + n * B_{counter}$$

n is the number of delay cell, B_{coarse} is the sampling binary code while $B_{counter}$ is the binary code stored in the counter. We design the delay line with 8 delay cells and set every delay cell's delay time to be 4ns, the rising and failing edge of START signal propagate alternately through the delay line. The counter we used is 6 bits. The dynamic range of coarse stage can be infinite theoretically, in fact, the dynamic range is limited because of error accumulation and nonlinearity in the delay line. The proposed TDC in this paper can achieve the dynamic range of 1.5 μ s after simulation. Compared with the research results of recent years, 1.5 μ s is a very excellent dynamic range while most of them achieve a dynamic range of hundreds of nanoseconds.

The middle stage used a traditional delay line which consists of 16 delay cells with the resolution of 250ps and dynamic range of 4ns.

Figure 5. Coarse stage architecture

3.2 Dual-DLL

Traditional DLL has a single delay line, the precision is T_{CLK}/n , while T_{CLK} is the period of reference clock and n is the number of delay cells. In order to control the delay time of two delay lines of

VDL, a dual DLL structure is proposed as shown in Figure.6[6]. Dual DLL contains a fast DLL and a slow DLL, the fast DLL has shorter delay time while the slow one has longer. Each DLL consists of VCDL, PFD, CP and LP. When there is a phase difference between CLK_IN and CLK_OUT exist, the PFD generate UP or DOWN signal to control the charge pump, then the charge pump generates a control voltage to decrease or increase the delay time of the delay cell until the two signals are in phase.

Figure 6. Dual DLL architecture

As shown in Figure.6, the fast DLL contains n delay cells, when CLK_IN and CLK_OUT are in phase, the delay time of every delay cell can be determined as $\tau_f = T_{CLK}/n$. We chose the $(n+1)$ th output of the fast delay line to match the n th output of the slow delay line. It forces the delay time of slow DLL to be:

$$n * \tau_s = (n + 1) \tau_f \quad (1)$$

$$\tau_s = \left(\frac{T_{clk}}{n} \right) * \frac{n+1}{n} = T_{clk} * (n + 1)/n^2 \quad (2)$$

This architecture has an important advantage that such a Dual-DLL needs only a single reference clock instead of two.

3.3 VDL architecture

The Dual-DLL we proposed before works for the fine quantization stage, VDL, shown as Figure.7. Obviously, the VDL architecture contains two tapped delay line with different delay time. Besides, the number of delay cells in VDL should be the same as in Dual-DLL. The resolution of the VDL architecture is determined as:

$$\tau_{VDL} = \tau_s - \tau_f, \text{ while } \tau_s > \tau_f.$$

Figure 7. VDL architecture

The delay time of the two delay lines are controlled by the voltage provided by the Dual-DLL. According to the delay time determined above, fine quantization resolution is:

$$\tau_{fine} = \tau_s - \tau_f = T_{clk} * \frac{n+1}{n^2} - \frac{T_{CLK}}{n} = T_{CLK}/n^2 \tag{3}$$

In this paper, the reference clock is 125MHZ and n is 32, $\tau_{fine} = 7.8125ps$. The dynamic range of fine stage is $7.8125ps * 32 = 250ps$, which matches the resolution of middle stage.

4 Circuit description

This section describes the circuit scheme of some typical blocks.

4.1 Delay cell

We set the delay time of delay cell in coarse stage to be 4ns. The schematic of the delay cell with bias we chose is shown in Figure.8. It contains 3 nMOS and 3 pMOS, the voltage V1 and V2 is used to control the delay of rising edge and failing edge. The delay time can be set to be 4ns by changing the ratio of width and length of MOS.

The delay cell of the middle stage uses the same architecture above. Figure.9 shows the schematic of delay cell in fine stage[7]. The difference is that there is only one control voltage to control the delay of rising edge. Obviously, the control voltage here is generated from DLL we described before.

Figure 8. Schematic of the delay cell in coarse stage

Figure 9. Schematic of the delay cell in fine stage

4.2 Symmetrical DFF

There is a set of DFFs match the delay cell in every quantization stage to sample the propagation state of target signal. The difficulty in designing the DFF lies in providing the same path for two signals propagate through DFF, so that the delay time of these two signals are the same, there is no extra error been brought in. That means we need a symmetrical DFF and its schematic shows as Fig.10.

Figure 10. Symmetrical DFF

4.3 Control structure for DLL

The main problem of DLL is fail to lock or falsely lock to two or more periods. In order to make DLL lock correctly, we proposed a control structure for DLL shown as Fig.11 and Fig.12, and the former is for the fast DLL while the latter is for the slow DLL.

Take Fig.11 for example. A rising edge of SETUP signal generated when the first failing edge of REF_CLK comes, the first rising edge of REF_CLK is ignored so that the DFF won't fail to lock. The timing diagram is shown in Figure. 13.

Figure 11. Control structure for the fast DLL

Figure 12. Control structure for the slow DLL

Figure 13. Timing diagram

5 Simulation and conclusions

The designed circuit is tested in Cadence Spectre software using SKYSILICON Co.Ltd CD035MVA 0.5μm CMOS process, and the simulation result of Dual-DLL is as Fig.14. The fast DLL costed 460.9ns to be stable while the slow DLL costed 582.6ns. The control voltage generated to control fast line and slow line of VDL are 1.798V and 1.59V.

Figure 14. Simulation of Dual-DLL

We have proposed that the resolution of the fine stage is 7.8125ps, but the actual resolution from the simulation result shows 8ps~9ps, the error exist because the architecture of DLL will bring in some phase error, the propagation route of START and STOP signals in delay line can't be exactly the same, and even the DLL is locked, the jitter of control voltage still exists.

In this paper, a high-precision TDC using a three-level conversion scheme was proposed. With the development of integrated circuit technology, a TDC with both high resolution and wide dynamic range is need, only achieve one target is not enough. Compared with recent years' research results shown as Table.1, the TDC proposed in this paper performed well in the ratio of resolution and dynamic range.

Table.1 Recent years’ research results

Year	Paper	Precision/Dynamic Range
2013	A 7 bit, 3.75 ps Resolution Two-Step Time-to-Digital Converter in 65 nm CMOS Using Pulse-Train Time Amplifier.	3.75ps/480ps
2013	A high-linearity, 17 ps precision time-to-digital converter based on a single-stage Vernier delay loop fine interpolation.	17.2ps/160ns
2014	A 15b, Sub-10ps resolution, low dead time, wide range two-stage TDC.	8.125ps/204.8ns
2017	This paper	8ps/1.5μs

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