A Low-voltage Programmable Frequency Divider with Wide Input Frequency Range

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Abstract. A low-voltage programmable frequency divider with wide input frequency range is fabricated in standard 0.18 μ m TSMC RF CMOS technology and presented in this paper. Considering the frequency division ratio of dual-modulus prescaler is relatively smaller, a programmable divider with full custom design is used to increase the frequency division ratio and the maximum operating frequency. The frequency division ratio of the programmable frequency divider covers from 64 to 255. And the measured results show that the programmable divider works correctly when the input frequency varies from 0.5 GHz to 6.0 GHz, with 1V supply. Besides, the power consumption is 3.5 mA at the maximum frequency of 6.0 GHz.

1 Introduction

With the rapid development of wireless communication, various kinds of wireless communication mode are springing up constantly, making the integration of a variety of wireless communication in a mobile terminal a development tendency. The RF transceiver which supports multiple standards also therefore becomes a research hot spot. Many domestic and foreign scholars have made a thorough research about multi-mode multi-frequency broadband frequency synthesizers [1-3] which is indispensable in a multi-mode RF transceiver.

The programmable frequency divider as a critical module in multi-mode multi-frequency frequency synthesizers, is required to work under the broadband and high frequency [4-5]. Because of the simple structure, the programmable frequency divider made up by dual-modulus prescaler and programmable divider is extensively applied. The programmable counter is constituted by a *Programmable* counter (P-counter) and a *Swallow* counter (S-counter). Usually, the two counters are designed by semi-custom design approach, which can only work at a low frequency band. In order to obtain a higher working frequency, the counters presented in this paper are designed by full custom design approach. At the same time, the frequency division ratio of dual-modulus prescaler is designed to be small to lower the minimum frequency division ratio of the whole programmable frequency divider. So, the programmable frequency divider presented in this paper also has a large frequency division ratio range.

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2 Circuit design

2.1 Architecture of programmable frequency divider

The architecture of the programmable frequency divider is shown in Figure 1. The full programmable divider used in this design is based on the pulse-swallow topology and it contains a 8/9 (N/N+1) dual-modulus prescaler, a 5-bit P-counter and a 3-bit S-counter [6]. Signal DMPout is the output signal of the dual-modulus prescaler (DMP). Signal DIVout is the final output of the whole programmable frequency divider. The total division ratio (TD) is given by

$$TD = S(N + 1) + (P - S)N = PN + S,$$
(1)

where P and S are the loaded initial values in the P-counter and S-counter, respectively. Equation (1) states that the programmable frequency divider presented in this design can cover the consecutive division ratio from 64 to 255.

Fig. 1. Topology of programmable frequency divider.

Fig. 2. Swallow counter.

2.2 Programmable divider

The 3-bit swallow S-counter used in the programmable divider is shown in Figure 2. It consists of three asynchronous loadable bit-cells, a DFF and logic gates to achieve programmability from 0 to 7. The asynchronous loadable bit-cell, as shown in Figure 3 is similar to the bit-cell reported in [7], except the five transistors M1 M5 M6 M9 M14 whose inputs are controlled by the logic signal SP or SPB. SPB is inversed to SP and when SP is

switched to logic ‘1’, S-counter stops counting. When the S-counter finishes counting down-to-zero, SP switches to logic ‘1’ and MC switches to logic ‘0’, then the precaler changes to the divide-by-9 mode for the left (P-S) clock cycles [8]. The S-counter can work correctly whatever the loading value is.

Fig. 3. Bit-cell used in S-counter.

Fig. 4. Programmable counter.

The 5-bit programmable P-counter used in the fully programmable divider is shown in Figure 4 [8]. It consists of five asynchronous loadable bit-cells, a NOR-embedded DFF and logic gates to allow it to be programmable from 2 to 31. The bit-cell used in the P-counter is similar to the bit-cell reported in [7] with optimized transistor size for low power consumption. When the P-counter finishes counting down-to-two, LD switches to logic ‘1’ and keeps the state for a clock cycle. It makes sure that bit-cell have enough time to load new counting value [9]. The NOR-embedded DFF shown in Figure 5 can be reset by the signal Reset. When Reset switches to logic ‘1’, LD switches to logic ‘1’ and both P-counter and S-counter load the new counting values. Note that the P-counter can work correctly when the loading value is not less than 2. Beside, in this design, the loading value of P-counter is not less than 8.

Fig. 5. NOR-embedded DFF with reset function.

2.3 Dual-Modulus prescaler

Fig. 6. Dual-modulus prescaler.

The prescaler as shown in Figure 6 employs a synchronous 4/5 dual-modulus divider and an asynchronous divider. The synchronous divider is constructed by three DFFs and two OR logic gates. When the mode control signal CONTROL switches to logic ‘1’, only DFF1 and DFF2 are working in fact. So signal Q2b of DFF2 feedback to DFF1, consequently the synchronous divider divides the signal clk by 4. When the mode control signal CONTROL switches to logic ‘0’, Q3bn+1=Q2bn and Q1n+1=Q2bn|Q3bn. So the synchronous divider divides the signal clk by 5.

In this design, source coupled logic (SCL) circuit as shown in Figure 7 is chosen as the DFF [10]. To increase the operating frequency and save the power consumption, the OR logic gate is integrated in the SCL circuit directly [10], as shown in Figure 8. Asynchronous divider is constructed by True-signal-phase-clock (TSPC) circuit [11] and it divides the signal from the synchronous divider by 2. When MC switches to logic ‘0’, the division ratio of prescaler is $2 \times 4 = 8$. When MC switches to logic ‘1’, in a whole dividing cycle, the prescaler divides clk by 8 for 0.5 cycle and divides clk by 10 for the other 0.5 cycle, so the division ratio of prescaler is $8 \times 0.5 + 10 \times 0.5 = 9$.

Fig. 7. SCL circuit.

Fig. 8. SCL circuit integrated with OR logic gate.

3 Simulated results

The layout of the programmable frequency divider is shown in Figure 9. It consists of a S-counter, a P-counter and a dual-modulus prescaler. The area of the whole circuit is 0.258 mm×0.168 mm.

Fig. 9. Layout of the proposed divider.

The post simulation is performed in Cadence. When the frequency is 6.5 GHz, the inputs and outputs of the prescaler are shown in Figure 10. According to the markers placed in the waveforms in Figure 10, we know the division ratio is 8/9 by simple calculation. The prescaler can work correctly with 0.5-6.5 GHz input range and consumes 3.19 mA when the frequency is 6.5 GHz and supply voltage is 1V.

Fig. 10. Post simulated prescaler input and output waveforms.

Fig. 11. Post simulated programmable frequency divider input and output waveforms.

The post simulation result of input and output of the whole programmable divider is presented in Figure 11. The counting value of P-counter is 8 and the counting value of S-counter is 1, so the division ratio of the whole programmable divider is 65, as calculated by Equation (1). In the Figure 11, the first waveform is the input signal clk , whose frequency is 6.5 GHz, the second waveform is the output signal $DMPout$, the third waveform is MC , and the fourth waveform is the output signal of the whole programmable divider $DIVout$. According to the markers placed in the waveform in Figure 11, the division ratio is 65, which is consistent with the value calculated by Equation (1). The highest frequency that P-counter and S-counter designed by the full custom approach can work at is around 900MHz. The programmable divider can work correctly with the input range of 0.5-6.5 GHz. And it draws 4.99 mA current from 1V supply voltage at the maximum frequency.

4 Measured results

The proposed programmable divider is fabricated using standard 0.18- μm CMOS technology with six metal layers. The whole circuit (including pads) occupies a chip area of 0.675mm $\times$ 0.378mm, and the die micrograph is shown in Figure 12.

The measured results of input and output of the whole programmable divider is illustrated in Figure 13. The counting value of P-counter is 16 and the counting value of S-counter is 4, so the division ratio of the whole programmable divider is 132, which is

calculated by Equation (1). The frequency of input signal clk is 6 GHz. In Figure 13, the first waveform is the output signal of the whole programmable divider DIVout, whose frequency is 45.45 MHz ; then, the second waveform is the output signal MC ; finally, signal DMPout is shown in the third waveform. Figure 14 shows the output frequency spectrogram of the programmable divider. According to the data in the waveform in Figure 13, we can obtain that the division ratio is 132. The measured results states that, when the input frequency varies from 0.5 GHz to 6.0 GHz, the programmable divider can work effectively. With 1V voltage supply, the consumed current is 3.5 mA at the maximum input frequency.

Fig. 12. Chip micrograph of the programmable frequency divider.

Fig. 13. Programmable frequency divider’s input and output waveforms.

Fig. 14. Frequency spectrogram of the output of programmable divider.

Fig. 15. Input sensitivity curve of the programmable divider.

Shown in Figure 15 is the input sensitivity curve of the programmable divider. As is seen in Figure 15, when the frequency of the input is 5 GHz, the required input power is minimum. Consequently, the programmable divider is most sensitive when the input frequency is around 5 GHz.

5 Conclusion

A 1V low-voltage programmable divider in standard 0.18 μ m TSMC RF CMOS technology is presented. The measured results show that the programmable divider operates correctly with the 0.5-6.5GHz input. At the maximum input frequency, a current of 3.5 mA is drawn from the 1V supply. The Input sensitivity curve of the programmable divider states that when the input frequency is around 5 GHz, the programmable divider is most sensitive and the required input power is minimum.

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