A IF Signal Precessing System Design Based on Software Radio Platform

Jing Zhao[1,*], *Hao* Nie[1], and *Jing* Yu[1]

[1]Aviation Maintenance NCO Academy of Air Force Engineering University Xinyang Henan, 464000, P. R. China

Abstract. Software radio is a definition of a design thought about how to implement flexible functions by using fixed hardware platform. Any platform based on this is characterized to be universal, standardized, modular, open and highly flexible. Due to some realistic reasons, a software radio platform is hard to be realized. So, most signal processing is operated after mixing. According to software radio requirements, a "FPGA+ADC+DAC" structure is designed. Compared with former processors, this module has broad application prospects with the small size, low power, configurable and programmable feathers. It has multifunction, such as generating IF signals, performing digital down conversion and realizing the synchronous demodulation and the other functions. This module also provides the extended host interface to communicate with upper computers. According to the practical test, take MSK signal for example, if the bit rate is 1Mb/s, bit error rate is lower than 10^{-6}.

1 Introduction

The main design philosophy of software radio [1,2,3] is to make A/D and D/A converter close to the antenna, if possible, and realize hardware functions with method of editing software, such as frequency selection, modulation and demodulation, data format conversion, encoding and decoding, communication protocols and so on. Considering the processing speed of DSP or FPGA and data storage capacity, normally, A/D and D/A converter only can be placed before intermediate frequency (IF) module. Currently, IF sampling software radio structure is widely employed into digital transceiver.

The classic IF transceiver structure is shown on fig. 1. It includes T/R switch, low noise amplifier, mixer, wide-band IF amplifier, power amplifier, wideband filter and digital signal processing.

For the digital signal processing, it might be implemented by ASIC, DSP and FPGA. To a software radio system, ASIC is no longer suitable in system design because it is detrimental to module interchangeability and increases the system complexity and power consumption. Early SDR platform generally uses DSP as the core processor, but the DSP line mode reduces the system parallelism. Afterward, the structure of FPGA+DSP is used to improve the real-time and parallel processing capabilities instead of DSP. However,

* Corresponding author: sherilljames@163.com

differences between FPGA and DSP work mode will make it a long time to transfer the data between them. With the increase of data processing capacity in communication systems, data transmission between FPGA and DSP will have more influence over the processing speed of the whole system. Therefore, FPGA used as the system processor is a development trend of SDR structure.

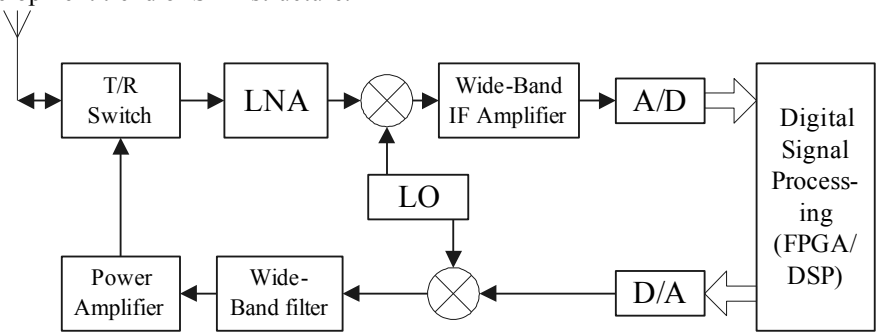

Fig.1. IF Transceiver software radio structure

In this paper, the hardware structure of ADC+FPGA+DAC is applied, and a common host interface is designed to extend the functionality. Its block diagram is shown on fig. 2.

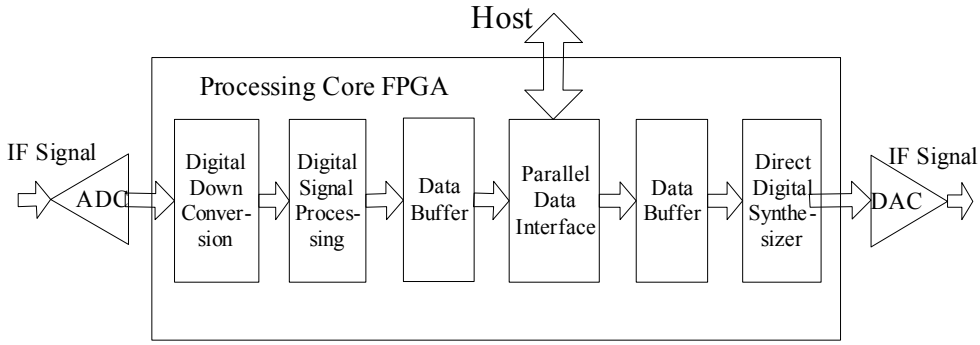

Fig.2. System structure

In this way, the signal processing could be adopted for many communication systems, such as ASK, MSK, PSK, MSK and DQPSK etc.

2 System realization

In the system, the Xilinx FPGA XC2V3000, ADI's ADC AD9430 with maximum sampling frequency 210MHz, and ADI's DAC AD9753 with maximum sampling frequency 300MHz are applied. Taking MSK IF signal for example, analyze its realization process.

MSK is minimum frequency shift keying. It is a binary frequency shift keying signal with minimum bandwidth. So, it is widely used in digital communication systems. To demodulate MSK IF signal, the system might have digital direct synthesis (DDS), down digital down conversion (DDC), synchronous (coherent) demodulation etc.

Fig. 3 shows the FPGA internal signal processing flow chart. According to DDS theory, FPGA controls DAC to generate the MSK IF signal and deliver it to the ADC front-end of this module through analog channel. According to the bandpass sampling theorem, FPGA controls ADC to sample the MSK signal and transmits the results to the host through the communication interface after digital down conversion, demodulation, frame alignment,

parity check, and so on. Firstly, the sampled data is transmitted into the DDC unit through the registers; secondly, the baseband signal is extracted above to mixer and low-pass filter to complete the MSK demodulation; thirdly, FPGA performs the frame alignment and parity check; finally, the processing results is buffered into RAM so as to transmit to host.

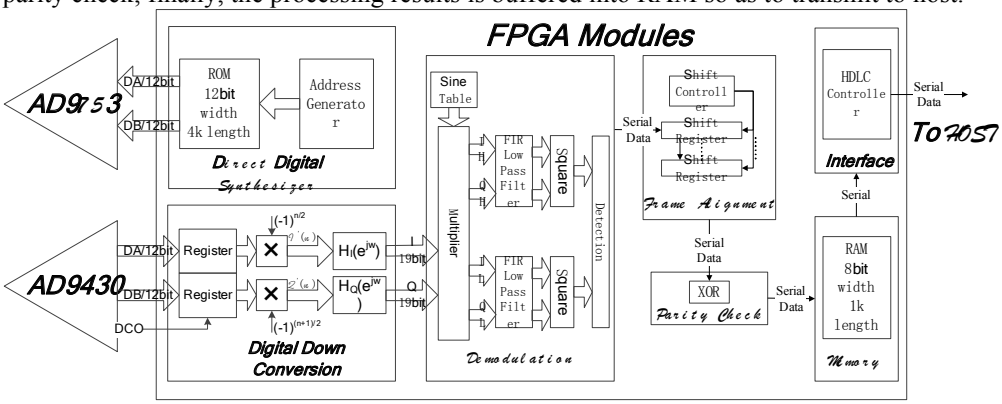

Fig. 3. FPGA internal signal processing flow chart

2.1 DAC control

The AD9753 is a 12-bit dual digital input digital-to-analog converter. Since the internal Phase-Locked Loop (PLL) circuitry is able to double frequency of input clock, the two input digital data is converted to analog signal at twice the speed of the input clock and sent out. Therefore, FPGA can control the DAC using half the sampling frequency.

Two 12-bit wide, 4096 deep read-only memory (ROM) is generated inside the FPGA, which stores 4096 sampled single cycle sinusoidal wave data. According to DDS theory, we can get the frequency control word K. Two memories take 0 and K as the initial address respectively and $2K$ as the increment address. FPGA inputs the clock signal at half of the sampling frequency to DAC in the differential form through the clock chip MC100LVEL16. At this rate the data read from two memories is sent to the P1B and P2B port of DAC. The DAC output analog signal becomes a single frequency signal through low-pass filter and amplifier circuit.

We can get signals of different frequencies according to different control word K and do the coding combination of the two signals on the basis of sending codeword required, thus, the transmission of MSK signal is realized.

2.2 ADC sampling control

AD9430 is a 12-bit dual digital output analog-to-digital converter. Since the internal clock management circuitry is able to divide frequency of input clock by two, the output data at half the speed of the input clock is latched and then transmitted to the processor. Therefore, FPGA can do the data processing using half the sampling frequency.

MSK IF signal becomes a differential signal after the transformer, and then is input to the ADC. Meanwhile, FPGA generates the sampling clock and input it to the ADC in differential form through the clock chip MC100LVEL16. ADC sends the sampling data to FPGA through digital ports DA and DB and divides sampling frequency by two simultaneously, which is provided to FPGA in differential form as data synchronous clock DCO. The data of ADC is assigned to the internal registers for digital down-conversion by FPGA on falling edge of DCO.

2.3 Digital down conversion (DDC)

As the data sampled by AD9430 is two parallel output, the parity extraction of the FPGA input is not necessary. The input data from port DA and DB is regarded as I Road and Q Road signal directly. By taking the opposite sign of another I signal point and another Q signal point respectively, the processing of signal multiplied by $(-1)^n$ is realized.

By eight parallel multiplier and an 3-level adder with 8-input, 1-output, we can obtain the eight-band FIR filter. Two sets of filter coefficients are designed with the phase delay difference of $2\pi/T'$. Then, I signal after the filter is delayed $T'/2$ sampling period more than Q signal, thus, the time alignment of I Road and Q Road is realized.

In the process of implementation, we change the sampling frequency as $f_S = 4f_L/3$. From the preceding analysis, f_H becomes $2\Delta f$ and f_L becomes direct current (DC) signal after DDC processing. Then, only the mixing of $2\Delta f$ is necessary to be processed inside the FPGA, saving the FPGA internal resources of multipliers and logic units.

2.4 MSK demodulation

Since the low frequency signal has been converted into DC signal in the process of ADC sampling and DDC, the demodulation is divided into two parts, as shown in Fig. 4.

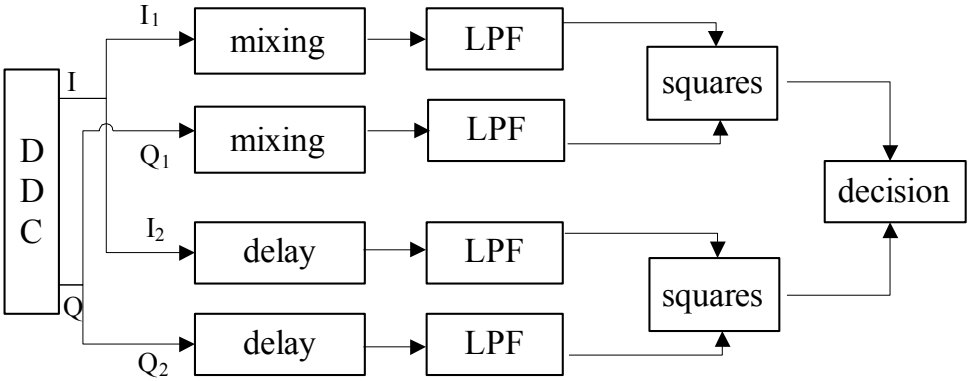

Fig. 4. MSK demodulation block diagram

A memory is generated inside the FPGA, which stores a sampled single cycle sinusoidal wave data. Then, by reading data from the memory at the processing-frequency, the look-up table method is realized and local oscillator (LO) signal at frequency of $2\Delta f$ is generated. After I1, Q1 and the LO signal above are mixed in the Mixer, frequency components are DC, $2\Delta f$ and $4\Delta f$ respectively. To ensure that four signals are sent into the LPF simultaneously, the I2 and Q2 signals go through the Delay Line Device with the same processing time as the Mixer.

After that, we generate a FIR low-pass filter by using the same method as polyphase filter and change the specific coefficient in order to make the cut-off frequency be 500 KHz. After the LPF, the high frequency components are filtered and only the DC component is retained. Take the sum of squares of the DC components of I1and Q1, I2 and Q2 respectively to get the amplitude information of MSK signal components with two frequencies. Then, the MSK symbol is achieved by joint judging the amplitude values.

2.5 Frame alignment

After the video symbol is obtained, the data symbol alignment and frame alignment is processed. For frame alignment, the matching method uses shift-register. We assume the symbol length of frame header is N, and then M shift-register with N-bit is constructed inside the FPGA. When the input symbol is detected, start the current register and prepare the next register at the same time, and then start the M shift-registers successively and circularly. Judge the register before each shift, if the symbol of any register is exactly the same as specified frame header before, the frame alignment is successful; otherwise, keep shifting until it is successful. The process of frame alignment is given in Fig. 5.

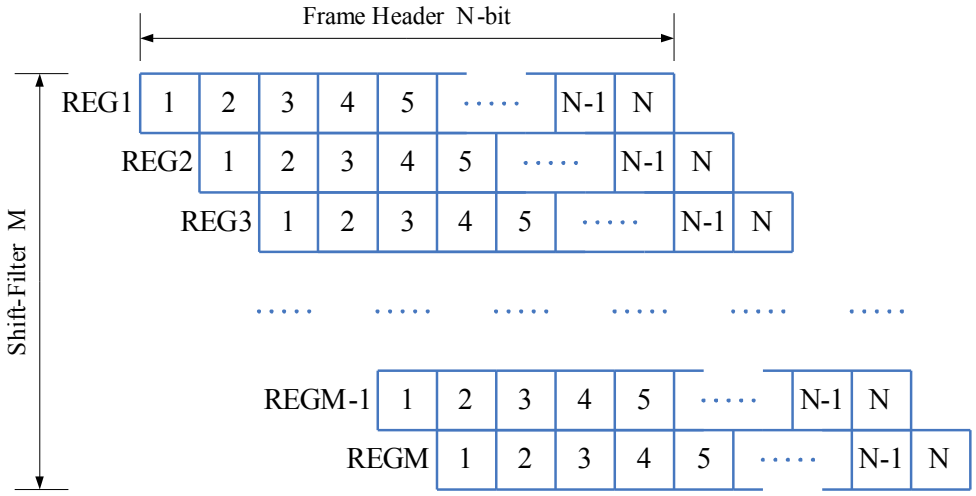

Fig. 5. Process of frame alignment

2.6 Data processing and transmission

After the success of frame alignment, the MSK data is collected according to timing relationship of the data frame. Then we decode each group of collected data, including removing the prefix, suffix and parity bit, and so on. Do the bitwise operation XOR to the data decoded and, compare the results with the parity bit. If both are the same, the data is judged to be valid and is stored in the FPGA internal memory in the form of bytes. If not, discard this frame of data and send an error report to the host.

To communicate with the host, we generate a SPI communication module inside the FPGA and do the optical coupling isolation and voltage conversion by convert devices on the communication interface. The host sends the encoded data and corresponding request through SPI interface. The SPI communication module receives the encoded data and sends the MSK data to be stored and error report to the host according to the command.

3 System test

During the test, we set the parameters as follows: IF 120MHz, bandwidth 10MHz, signal rate 1Mbps, frame rate 100fps, and take the MSK signal output of the module as the IF signal input of the module, the communication rate 2Mbps. The test time is 30 hours and the number of frame tested is 107.

Fig. 6. comparing results

The comparison of the output MSK symbol and input MSK signal results is shown in Fig. 6.

After the actual test, the delay of output symbol is 1.05μs. When the signal-to-noise (SNR) of the input IF signal is greater than 10dB, the bit error rate (BER) of MSK demodulation is better then 10-6 and the bit error rate (BER) of communication is better then 10-6, meeting the general requirement of wireless communications.

4 Conclusion

According to the idea of SDR, the MSK communication module of ADC+FPGA+DAC is designed in this article, including the bandpass sampling and the generation of the IF MSK signal. The data processing such as DDC, polyphase filtering and MSK demodulation is realized inside the FPGA. As the system is based on the SDR architecture of broadband IF sampling and all of the signal controlling and data processing is realized in one FPGA, it can meet the requirement of various communication systems by modifying the hardware program. Since digital down conversion is applied in the course of signal sampling, the processing of IF signal at higher carrier frequency can also be achieved. The system has good versatility and reconstruction, with a broad application prospects.

References

1. Alsliety, M., Aloi, D.N. Signal processing choices and challenges for SDR in Telematics [J]. International Symposium on Signal Processing and Its Applications, Feb. 2007, pp1-4.
2. Hatai, I., Chakrabarti, I. FPGA implementation of a digital FM modem for SDR architecture [J]. International Conference on Computer and Devices for Communication, Dec. 2009, pp1-4.
3. Zhao DeAn, Lian XianGuo and Yang Ping. Multi-rate Signal Processing for Software Defined Radio (SDR) and Realize on FPGA [J]. International Forum on Computer

Science-Technology and Applications, Dec. 2009, pp251-254.
4. Pan Yun, Ge Ning and Dong Zaiwang. Mixed-Signal Modeling and Analysis for a Digital RF Direct Sampling Mixer [J]. IEEE International Conference on Circuits and Systems for Communications, May 2008, pp623-627.
5. Jie-Cherng Liu. Bandpass sampling of multiple single sideband RF signals [J]. International Symposium on Communications, Control and Signal Processing, March 2008, pp863-866.
6. Yamamoto, T., Kasahara, M. and Matsuura, T. A 63-mA 112/94-dB DR IF bandpass Modulator with direct feed-forward and double sampling [J]. Custom Integrated Circuits Conference, Dept. 2007, pp61-64.
7. Mitola, J. The software radio architecture [J]. IEEE communication magazine 1995 Volume 33, Issue 5,pp26- 38.
8. Zhang Rui, Li Jiandong. A New Type of Practical Software Radio Architecture [J]. ACTA EL ECTRONICA SINICA, Nov.1999,pp39-41.
9. Zhang Jianli, Yang Jiawei, Huang Pengyu. Study And Realization Of A Software Radio IF Modulation demodulation Platform Based On Dual DSPs [J]. Space Electronic technology, S1,2006,pp158-162.
10. Wei Zheng, Zhou Chunhui Zhao Ming. Software Radio Platform Design Based on High-Performance DSP [J]. Microcomputer Information, 02.2007, pp198-200.