Simulation and experimental model of power electronics UPS converter with the possibility of active parallel compensation

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Abstract. In the article the elaborated simulation and experimental models of the power electronics UPS converter with the possibility of active parallel compensation were described. The power circuits, control algorithms and the principle of working of presented UPS structure were presented. Also the chosen simulation and experimental results were analyzed.

1 Introduction

The work presents a structure of a power stage and a control system of the one-phase UPS with VFI structure [1], which additionally has an ability to compensate phase shift between fundamental harmonics of the voltage and current in power grid and reduction of higher harmonics generated by other energy loads connected to the common grid's node.

Phase shift compensation for the described UPS depends on the consumption of current with the opposite phase angle in relation to the resultant current drawn by other loads. The function of higher harmonics compensation forces the input current of the UPS to be deformed in the manner that its sum with the currents of the cooperating loads gives the resultant signal, which is characterized by the lowest possible content of undesired harmonics in the considered frequency band.

1.1 Operating principle of the UPS

The block diagram of the system is presented in Fig. 1. The UPS is powered from a power grid together with the other loads. Loads which needed a high parameters supply are powered from the UPS.

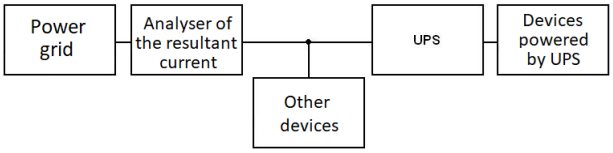

Fig. 1. Simplified block diagram of electrical system with UPS, cooperating with other loads connected to power grid.

The input stage of the UPS was designed on the basis of a fully controllable transistor bridge with an induction filter [2]. The DC/DC impulse converter, which enables the charging of a battery pack, is based on the DC/DC BUCK converter [3]. The output module operates as a closed-loop control system and worked as a controlled voltage source. The block diagram of the UPS with VFI structure is presented in Fig.2.

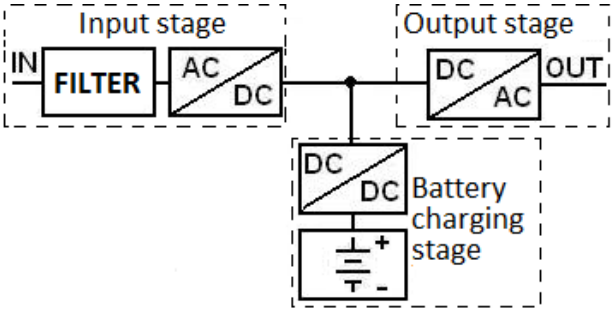

Fig. 2. Block diagram of the UPS based on VFI structure.

2 Structure of the UPS input stage

2.1. Simulation model

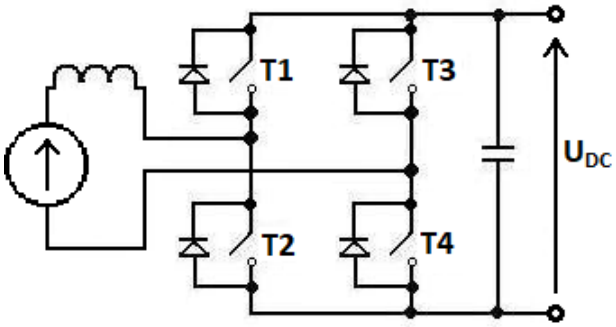

Fig. 3. Diagram of UPS input stage.

The task of the UPS input stage in the described solution is stabilization of the voltage on the DC bus and active phase shift and higher harmonics compensation of the resultant grid current.

The proposed solution does not need to use additional modules in the form of passive or active filters to improve the quality of the grid current [4, 5].

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The block diagram of the control system of the UPS input stage is presented in Fig.4. A master PI voltage regulator on the DC bus was used. As a slave regulator, the PI current regulator was implemented [6].

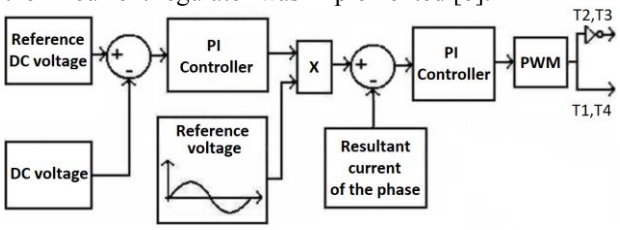

Fig. 4. Block diagram of the control system of the UPS input stage.

2.2 Experimental model

The input stage of the UPS was designed on the basis of ALFINE TIM's P3-5.0/550MFE LABINVERTER [7] with additional input choke. The block diagram of the LABINVERTER is presented in Fig. 5.

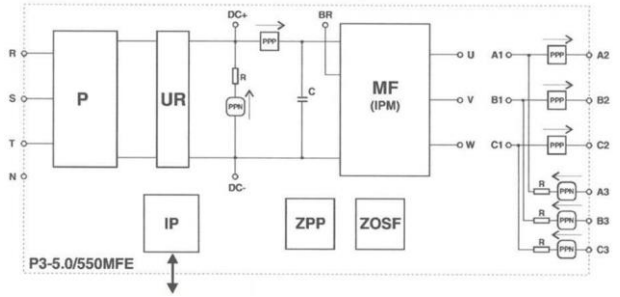

Fig. 5. Block diagram of P3-5.0/550MFE LABINVERTER.

The converter is based on two power electronics components: a three-phase integrated diode rectifier (P) and a 3-phase intelligent power module with Mitsubishi's PM50RSA120 IGBT keys, which is a component of the voltage inverter (MF) module. The input rectifier (P) was not used during the implementation of the laboratory model, just like the system (UR), which enabling pre-charging of the intermediate circuit capacitors. In the analyzed case, one leg of the MF module was not used.

The digital control system for the keys of the transistor rectifier was implemented based on the ALFINE TIM's ALS-G3-1369 evaluation board [8] with the Analog Device's third-generation SHARC signal processor family of type ADSP-21369.

3 Simulation and experimental researches results

Research of the UPS simulation model was carried out in the Matlab environment. A summary of the obtained simulation and experimental research results is presented in Fig. 6 and Fig. 7.

During the initial tests of the physical system, the function of active parallel compensation of the system was deactivated.

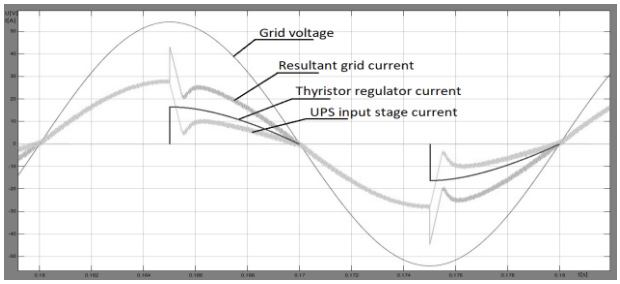

Fig. 6. Currents and voltage in power grid while additional load as thyristor rectifier with resistor at output.

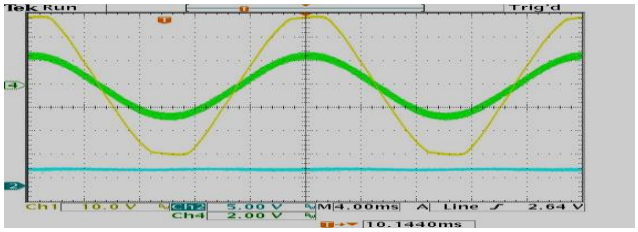

Fig. 7. Grid voltage (yellow signal), rectifier input current (green signal), and DC bus voltage (blue signal).

4 Conclusions

The paper presents the power and control stage of a one-phase UPS converter with the possibility of active parallel compensation. The use of such a solution makes it possible to reduce the investment costs associated with the installation of classic passive filters, or active parallel compensators.

References

1. S. Karve, Three of a kind [UPS topologies, IEC standard], IEE Review **46**, 27-31 (2000)
2. A. Dmowski, Warszawa, Wydawnictwo Naukowo-Techniczne, (1998)
3. K. Bednarek, and L. Kasprzyk, Pozn. Univ. Technol. Acad. J. Electr. Eng. **69**, 199-207 (2012)
4. E.W. Gunther, IEEE Transactions on Power Delivery **10**, 322-329 (1995)
5. F.Z. Peng, H. Akagi, and A. Nabae, IEEE Transactions on Industry Applications **26**, 983-990 (1990)
6. Z. Jędrzykiewicz, *Teoria sterowania układów jednowymiarowych*, (Kraków, Uczelniane Wydawnictwo Naukowo-Techniczne, 2004)
7. datesheet for LABINVERTER, Alfine TIM
8. datesheet for ALS-G3-1369, Alfine TIM