Evaluation of accuracy of SiC-JFET macromodel

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Abstract. In the paper, the results of experimental verification of the macromodel of UJN1208K JFET transistor made of silicon carbide fabricated by United Silicon Carbide, are presented. The macromodel form dedicated for PSPICE program is available on the manufacturer's website. The accuracy of the macromodel have been evaluated by comparison of selected calculated and measured static characteristics and C-V characteristics of the considered transistor. The influence of ambient temperature on the characteristics of the transistor has been evaluated, as well.

1 Introduction

Over recent years, technological progress in the field of semiconductor devices design has resulted in the appearance on the market of modern semiconductor power devices made of silicon carbide. This development trend also applies SiC-JFETs (Silicon Carbide Junction Field-Effect Transistors) often used in e.g. power electronics systems for generation and conversion of electrical energy [1-4].

Currently, in the process of designing and analysing of electronic circuits, appropriate computer programs containing reliable models of electronic components, are needed. In recent years, SPICE (Simulation Program with Integrated Circuit Emphasis) [5] has commonly been used as a comfortable CAD tool for the analysis of electronic circuits. A large number of passive and active devices models are built-in in SPICE, including a modified Shichman-Hodges [6] model of JFET.

On the other hand, semiconductor devices models (so-called macromodels) developed by manufacturers, are available, as well. A macromodel is formulated as an independent sub-circuit and contains e.g. SPICE built-in model, additional current or voltage controlled sources described by a suitable set of analytical dependencies, as well as additional passive devices [7].

In the paper, the form and principle of operation of the SiC-JFET UJN1208K macromodel offered by United Silicon Carbide [8, 9] are discussed. The accuracy of this macromodel was evaluated by comparison of calculated current-voltage and C-V characteristics with the corresponding characteristics included in the datasheet of the transistor. In addition, an influence of the ambient temperature on properties and characteristics of the transistor was investigated.

2 Results of simulations

The results of macromodel characteristics simulations of considered transistor were compared with the results of measurements presented in datasheet [9]. In subchapters 2.1 and 2.2, a current-voltage output characteristics and C-V characteristics of the transistor at different ambient temperatures are presented, respectively. Points denote the results of measurements, whereas the simulation results are denoted by solid lines.

2.1. Current-voltage characteristics

The output characteristics of the SiC-JFET at two arbitrarily chosen ambient temperatures for different values of the gate-source voltage are shown in Fig. 1 and 2.

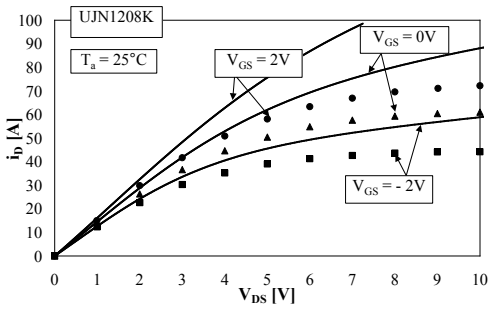

Fig. 1. Calculated and measured output characteristics of the transistor UJN1208K at 25°C.

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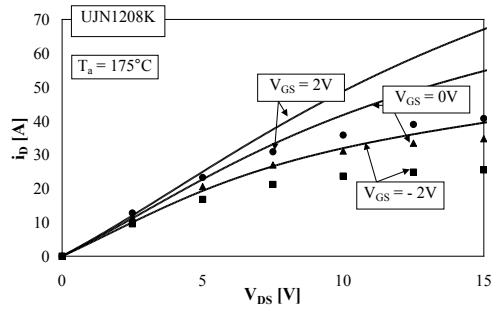

Fig. 2. Calculated and measured output characteristics of the transistor UJN1208K at 175°C.

As seen (Figs. 1 - 2), a good agreement between the results of simulations and measurements were obtained for the drain-source voltage not exceeding approximately 2.5 V at both considered ambient temperatures. For the higher values of the voltage V_{DS}, divergences between simulation and measurement results in the range from about 15% at temperature 25°C to even about 20% at 175°C, are observed, which indicates a high inaccuracy of the considered macromodel.

2.2. C-V characteristics

In the datasheet [9] of investigated transistor, C-V characteristics, such as: the input capacitance $C_{iss}(V_{DS})$, the output capacitance $C_{oss}(V_{DS})$ and the transfer capacitance $C_{rss}(V_{DS})$, are presented. The above mentioned capacitances express a suitable combinations of the transistor internal junction capacitances as follows [10]:

$$C_{iss} = C_{gs} + C_{gd} \quad (1)$$

$$C_{oss} = C_{ds} + C_{gd} \quad (2)$$

$$C_{rss} = C_{gd} \quad (3)$$

where C_{gs} - gate-source capacitance, C_{gd} - gate-drain capacitance, and C_{ds} - drain-source capacitance.

In case of simulations of C-V transistor characteristics, a special calculation circuits dedicated for SPICE [10], are used. An exemplary comparison of calculated and catalogue capacitance characteristics $C_{iss} = f(V_{DS})$ and $C_{rss} = f(V_{DS})$ of the SiC-JFET at fixed value of ambient temperature, are presented in Fig. 3.

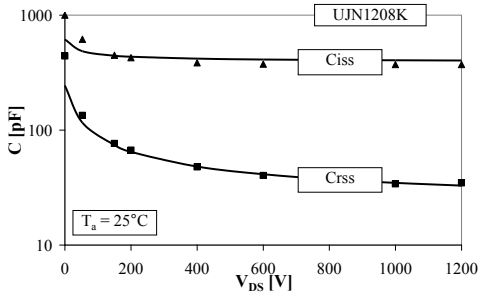

Fig. 3. Calculated and catalogue C-V characteristics of the transistor UJN1208K at 25°C.

As seen, a very good agreement between simulation and measurement results was observed, which proves the high accuracy of the macromodel in the case of transistor capacitance characteristics.

3 Summary

In the paper, evaluation of accuracy of the SiC-JFET macromodel of transistor UJN1208K is presented.
In the case of modelling of current-voltage characteristics, the considered macromodel is characterized by a relatively small accuracy, which leads to quite large discrepancies between the results of calculations and measurements.
On the other hand, a good agreement between the simulation and measurement results of C-V characteristics proves a high accuracy of the macromodel. In turn, the analytical description of the macromodel capacitance can presumably be used for modelling C-V characteristics of other JFETs made of silicon carbide.

References

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