

A fast switched reluctance motor controller based on FPGA

Daniel Rataj¹, Dennis Slawik¹, Krzysztof Wrobel^{1,*} and Krzysztof Tomczewski¹

¹Opole University of Technology, Faculty of Electrical Engineering Automatic Control and Informatics, Opole, Poland

Abstract. The paper presents the concept and practical implementation of a switched reluctance motor control system in an FPGA programmable device. The developed control system was designed for testing high-speed motors in order to limit the delays of output signals in relation to the signals from the encoder. The controller enables the values of commutation angles and PWM voltage to be set along with current limit values, measures the values of voltages and currents, and sends the results to the computer to be archived.

1 Introduction

Drives with switched reluctance motors (SRM) are characterised by a constant torque value over a wide speed range. However, achieving a high level of efficiency over the entire speed range requires the adjustment of commutation conditions to the machine's operating point [1]. Optimal relationships between rotational speed and commutation angles can be calculated using a mathematical model of the drive. The practical implementation of these relationships for high-speed drives is difficult, requiring the precise setting of output signals vs rotor position angle. Due to the rotor's high speed, the control system can cause delays resulting from the time required for calculations [2]. Therefore, when receiving high-frequency signals from the encoder, it may be necessary to limit their resolution. To avoid this, it is necessary to limit signal processing time; this is possible using hardware rather than software solutions.

2 SRM motor

The developed control system was designed mainly for testing a two-phase SRM drive, which had been optimised in terms of electromagnetic torque characteristics. The rotor of this motor is characterised by a non-cylindrical shape. The surface of the rotor teeth is described by 15 arches. The basic motor parameters are as follows: outer diameter of the stator magnetic circuit, 120 mm; package length, 80 mm; air gap diameter, 34.3 mm.

The characteristics of a drive with this motor obtained from the calculations are shown in Figure 1. According to the results of the simulation, the motor can operate over a speed range up to 18.000 rpm. In order to take measurements of its characteristics over the full speed range, it is necessary to minimise the time required to determine output signals.

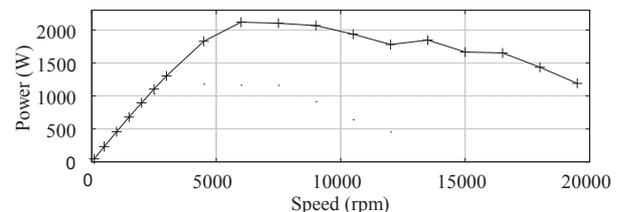


Fig. 1. The characteristics of the tested drive system as obtained from the simulation.

Determining the rotor position angle with an accuracy of 0.25 degree, at the maximum speed of the rotor, requires the calculation of outputs states at a frequency of 432 kHz. The execution time of the control algorithm must not exceed 2.3 μ s. The proposed control system was based on an FPGA programmable device. FPGA topology is designed for concurrent execution of multiple tasks [3, 4].

3 Control system topology

For the implementation of the control system, an Xilinx Artix-7 FPGA was used. The system enables the control of machines from 2 to 6 phases, and contains two main modules: control and measurement. The former carried out the motor control and user interface functions. The latter performed measurements of currents and voltages during the control process; at the same time, this module transmitted the measurement results to a computer via a USB interface. The computer program archives the results of measurements in a text file. Descriptions of the basic controller structures were made using the VHDL language in the Xilinx ISE environment; the control system synthesis was performed in the Schematics module. The control module includes a user interface block with a serial menu which used a four-button keyboard and an alphanumeric display.

* Corresponding author: k.wrobel@po.opole.pl

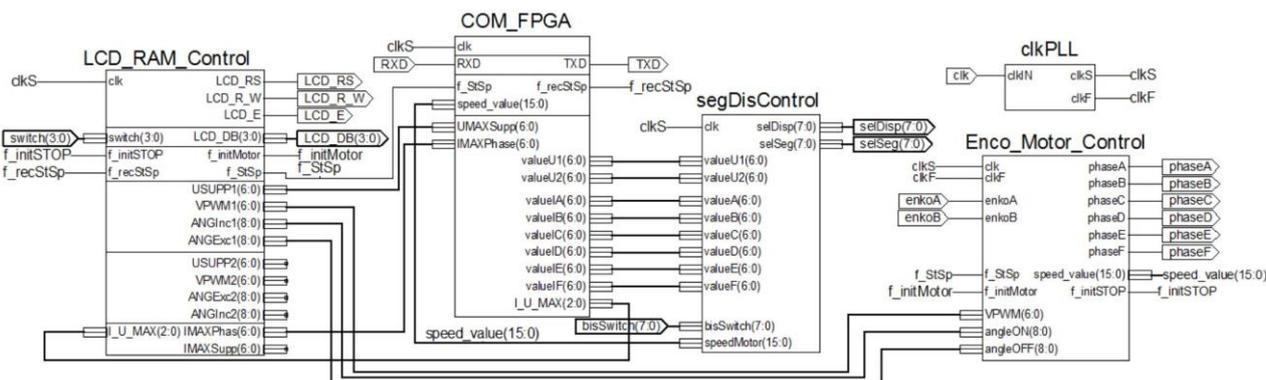


Fig. 2. Control module topology.

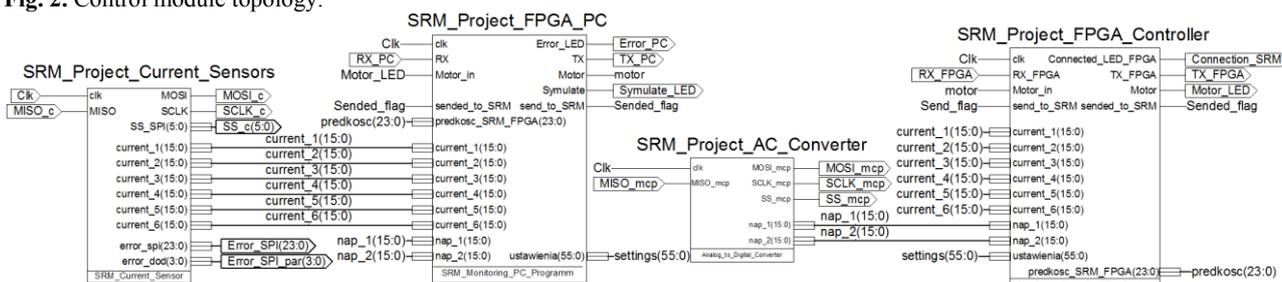


Fig. 3. Measurement module topology.

Due to the relatively large amount of data needed to operate the display, this module mainly uses the internal memory of the FPGA. Other modules, i.e. the central control system, PWM generator, current limit system, rotor position decoder, and control system of execution transistors, were based on the programmable structure and hardware DSP circuits. The developed architecture of the control module is shown in Figure 2.

The central control module was adapted to implement several SRM control algorithms intended for various power electronics systems.

To measure currents and voltages in the power electronics circuits, Hall sensors with ADC transducers with SPI output were used. Accordingly, the measuring modules `SRM_Project_Current_Sensor` and `SRM_Projekt_AC_Converter` were equipped with SPI interfaces with additional addressing outputs. These modules enable the measurement of 6 currents and 2 voltages. The measurement results are sent to the `SRM_Project_FPGA_Controller` control module via the UART interface. This solution was adopted because it enable the implementation of both modules in separate small FPGA devices. The second UART interface (`SRM_Project_FPGA_PC`), to which the USB converter is connected, was implemented for communication with the computer. In addition to the data archiving function, the computer program enable remote configuration and control of the system from a computer. The architecture of the measurement module is shown in Figure 3.

The maximal measured delay value of the output signal relative to the edge of the encoder signal was 406 ns. The UART transmission frequency between both main modules is 10 MHz, and between measurement module and the computer was 3 MHz.

At two-byte ADC measurement resolution with 1 byte label and 8 measured canals, as well as three-byte resolution with 1 byte label of rotor position angle or

speed measurement, the maximum data transfer speed via USB interfaces was 3300 records each 9 values per second.

The maximum delay from initialising a current measurement to changing the state of the output ports was 130 μ s. The results presented here refer only to FPGA structure, without peripherals such as drivers or power transistors

4 Summary

The developed structure makes it possible to execute the SRM control algorithm with delays shorter than the commutation time of the power transistors. This enables drive testing at very high speeds. The system enables the acquisition of measurement data such as currents, voltages, angular position of the rotor, and rotational speed. With a resolution of rotor position angle measurement of 0.25 degrees, the system can control a motor operating at 100.000 rpm.

References

1. K. Yasumura, Y. Inoue, S. Morimoto and M. Sanada, IEEE 12th International Conference on Power Electronics and Drive Systems, Honolulu, HI, 2017, 343-348
2. J. Gottschlich, B. Burkhart, C. Coenen and R. W. De Doncker, IEEE International Symposium on Sensorless Control for Electrical Drives and Predictive Control of Electr. Drives and Power Electr., Munich, 2013, 1-7
3. A. Stumpf, D. Elton, J. Devlin and H. Lovatt, 9th IEEE Conference on Industrial Electronics and Applications, Hangzhou, 2014, 12-17
4. H. Gürsoy, M. Önder Efe. IFAC-PapersOnLine **49**, 425-430 (2016)