

# Implementation of a rotor position determination system for a switched reluctance motor in FPGA devices

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**Abstract.** The paper presents three rotor position detection modules implemented in FPGA devices. The modules are characterized by different methods of implementation and were developed for use with a switched reluctance drive. They operate in the following modes: sequentially synchronized with a clock signal, concurrently synchronized with a clock signal, and asynchronously. Simulated and measured delays introduced by these modules in the FPGA device are presented.

## 1 Introduction

A switched reluctance motor (SRM) can achieve high rotational speeds, even in excess of 100,000 rpm. [1] Achieving a high level of accuracy in determining the angular position of the rotor for such speeds requires the use of fast control units. FPGA devices enable the implementation of a control algorithm at this high speed. [2] FPGAs enable the creation of specialized logic structures capable of implementing a concurrent control algorithm. In these application areas, they have an advantage over microprocessor systems. The aim of the project is to develop a switched reluctance motor controller that enables precise determination of the rotor's angular position within a wide range of rotational speeds. [3] These structures were implemented in an Artix-7 XC7A100T device.

The controller includes an user interface with four buttons and an LCD display showing the serial menu options. The menu contains basic configuration parameters and enables the editing of control parameters. The current speed and phase current values are shown on an additional display. The rotor angular position is determined by an incremental encoder with a resolution of 360 pulses per revolution, taking into account the detection of all signal edges in both encoder channels. This enables determination of the angular position of the rotor with a resolution of 0.25°.

Based on signals from the encoder, the controller produces control-algorithm-generating pulses that turn on the supply of phase windings. Delays introduced by the controller depend to a significant degree on the operation of this module. The controller enables voltage regulation by means of PWM modulation and by limiting the maximum current value. None of the additional functions carried out by FPGA affect increase delays in determining the angular position of the rotor.

## 2 Implementation of the rotor angular position detection module

In the controller, three different structures, designed to determine the angular position of the rotor and to generate signals that control the phase winding supply, were implemented and tested. The goal of the studies was to reduce the delays introduced by the controller. The first structure was implemented in the form of a single process, implementing the algorithm sequentially. The second structure was developed in the form of concurrent processes. Both structures were synchronized with an FPGA clock signal. The third structure acted asynchronously, reacting to all edges of two encoder channels.

### 2.1. The structure works sequentially and is synchronized with an FPGA clock signal

The structure consists of one process that sequentially checks signal states in both encoder channels. The signal states are checked successively with a frequency of 500 MHz. Eight conditions determine all possible current and previous states of both signals from the encoder. Fulfillment of the defined condition results in incrementing or decrementing the value of the counter. In addition, the flag value for the direction of rotation is determined. The counter value is limited to the encoder resolution using all edges in both channels. The result of the operation is transferred via an 11-bit bus to the comparator module defining the supply ranges of phase windings.

### 2.2 The concurrent structure is synchronized with an FPGA clock signal

Synthesis of this structure was performed in the graphics module. It contains three functional blocks, of which the

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first contains 4 processes, one for each edge of the two signals from the encoder which determine the direction of rotor rotation. The next four processes, on the basis of the direction and flag signals in two encoder channels, generate pulses for the duration of the clock signal. These pulses are fed through the logic module to the reversing counter. The counter output is an 11-bit bus to the module, determining the ranges for supplying the phase windings.

### 2.3 The structure works asynchronously

The third structure consists of 9 concurrently operating processes, of which 8 contain conditions for edge detection of signals from both encoder channels for each direction. Fulfilling one of the conditions results in setting a high state on a specific bit of one of the two 4-bit signals. Changing the state of the first signal causes incrementation, of the second decrementation of the angular position counter. After changing the value of the counter, both signals are reset.

### 2.4 Simulation results

Figure 1 presents the simulation results of the operation of the rotor position detection modules and counter update and determination of the supply ranges of phase windings. The modules were started by the falling edge of the enkoA signal from the encoder, and the output signals are connected to all tested modules: e1\_phaseA, e2\_phaseA, and e3\_phaseA.

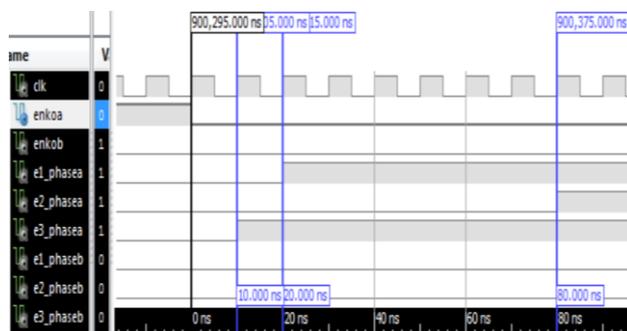


Fig. 1. Simulation results for rotor position detection modules.

After changing the input signal, the output of the asynchronous module was switched on first (after 10 ns). In the next step, the output of the module synchronized with the FPGA clocking signal working sequentially (after 20 ns). At the end, the output of the module synchronized with the clock running in parallel.

### 3 Measured results

In order to determine the actual values of the delays introduced by the position detection modules and the module that controlled the operation of the output transistors, the system was implemented in an FPGA device. The delay of output signals was measured in relation to the edge of the signal from the encoder. An

incremental encoder was connected to the Nexys 4 DDR module. Delays were measured using a Teledyne WaveSurfer 3054 oscilloscope with a 500 MHz measurement band. The modules were clocked with 100-MHz and 500-MHz signals.

Several measurement tests were carried out and the results averaged. For a clock frequency of 100 MHz, the following delays were obtained: for a module operating sequentially in synchronous mode, 41.9 ns; for a module operating concurrently in synchronous mode, 45.4 ns; for a module operating concurrently in asynchronous mode, 34.7 ns. At a frequency of 500 MHz, delays of 25.1, 23.33, and 22.89 ns were obtained, respectively, for these modules. The module that worked concurrently in asynchronous mode introduced the shortest delay. In subsequent tests, delays from 13.8 to 28.2 ns were obtained for this module.

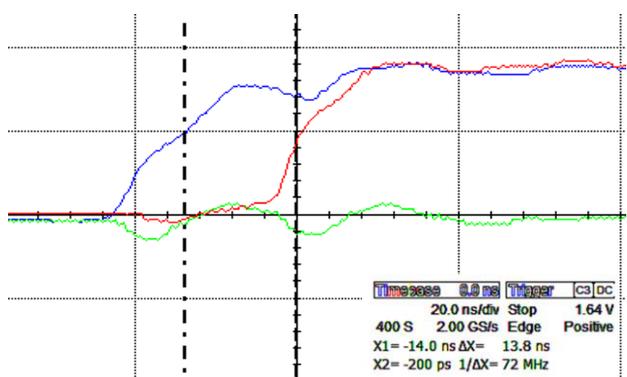


Fig. 2. Simulation results for the tested modules.

The delay introduced by the FPGA consisted of: time to determine the angular position of the rotor, to limit the value of the counter to the range of the encoder, and to determine the value of the output signals.

### 4 Summary

During the tests, the modules were implemented using neighboring Artix-7 ports. This operation enabled a twofold reduction in the delays introduced by the FPGA system in relation to the previously performed tests. [4] The best results were obtained for a system operating concurrently in asynchronous mode.

### References

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