

Particularities of complex-functional monolithic integrated circuits post-layout simulation

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Abstract. This paper presents a silicon-based complex-functional monolithic microwave integrated circuits (MMICs) design methodology. Post-layout simulation stage particularities are discussed. Pre-tapeout functionality verification results of the C-band phase and amplitude control MMIC based on 0.18 μm SiGe BiCMOS technology are also presented.

1 Introduction

Monolithic microwave integrated circuits (MMICs) are widely used in phased array radar and communication systems. Civil applications of phased arrays, in particular for the expected fifth generation (5G) telecommunication equipment, are limited by the complexity and the high cost of such systems [1].

Application of integrated circuits (ICs) based on silicon (Si) or silicon-germanium (SiGe) technologies can solve the problem of phased array systems high cost, especially in mass production. They are gaining popularity among system designers due to high level of integration and cost effectiveness in comparison with III-V semiconductor technologies.

The main drawback of Si-based devices is in high conductivity of substrate. It reduces the quality factor of passive components and increases the substrate coupling effects between circuit components. It also has negative impact on the noise performance of the circuit [2]. This leads to the necessity of the precise and at the same time high-performance simulation, especially for highly complex beamformer ICs (Core Chips).

Post-layout simulation becomes more and more challenging due to parasitic parameters, increasing along with the chip size. Design and simulation time does not necessarily correlate with complexity of the system. It really depends on the number of elements and circuit complexity.

Successful characterization of MMIC generally requires three different post-layout simulation steps: parasitic extraction, planar and full 3D electromagnetic (EM) simulation [3]. Interstage transmission lines and distributed structures cannot be modeled accurately using the quasi-static analysis used in parasitic extraction. Accurate designing and modeling of active and passive components, such as on-chip inductors, is highly challenging. EM analysis becomes an indispensable tool for characterizing the on-chip passive structures.

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In this regard, design methodology and results of post-layout simulation of the C-band phase and amplitude control MMIC based on 0.18 μm SiGe BiCMOS technology are presented in this paper.

2 MMIC design methodology

2.1 MMIC design flow

The main goal of MMIC design is to produce a working chip from the first tapeout. It is necessary to ensure that selected technology process is stable, accurate component models are provided by foundry, appropriate design methods are chosen. The design specifications should be met. MMIC should be tolerant to foundry process variations. It should occupy the smallest chip area in order to achieve high yield and low cost per unit. A typical IC design flow, including the proposed post-layout simulation stages, is shown in Fig. 1.

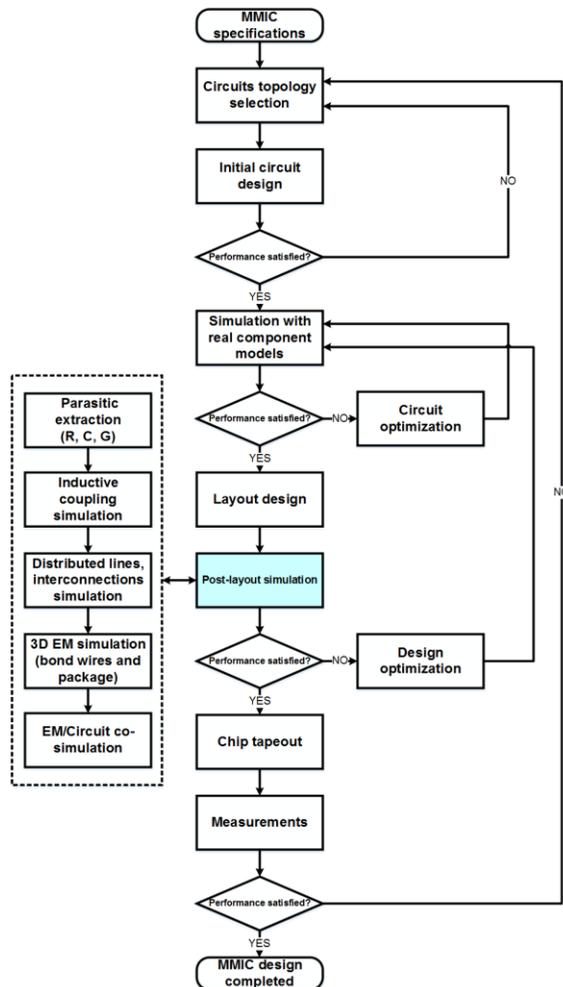


Fig. 1. MMIC design flow.

Complex-functional MMIC design starts with system level calculations and functional blocks topology selection based on initial specifications. It proceeds through component

level design, simulation, sensitivity and yield analysis and parameters optimization. Design process is iterative, as shown in Fig. 1.

After determining the required number of functional blocks and their topologies have been determined, appropriate circuit synthesis methods could be used. Electronic design automation (EDA) software tools usage is absolutely necessary for MMIC design process as it allows identifying and rejecting unrealizable circuit topologies quickly.

Once the MMICs component level circuitry has been designed and simulated it will usually require some form of optimization to satisfy specifications requirements.

The optimizer tool target parameters values should be chosen avoiding conflicting goals, for example, minimum return losses and minimum noise figure for low-noise amplifier (LNA) functional block. It is appropriate to start optimization process with simple circuits, narrow range of variables and component parameters that are agreed with the chosen technology. In case of a wide bandwidth of the designed MMIC several frequency points, such as the lower, the center and the upper could be chosen in order to reduce optimization time. Manual optimization is applied if the process trapped in a local minimum such that a global optimum was not obtained.

In the MMIC design, it is necessary to take into account foundry process variations, so that chip-to-chip differences still allow circuits to meet their specifications. The selected functional blocks topology should be insensitive to process variations. It is necessary to apply a process corner sensitivity technique, using for example EDA's parametric analysis tool.

If the circuit with real components models satisfies the specifications, the next stage would be MMIC layout design. While placing the components strict layout design rules such as minimum spacing between components, minimum component size etc. have to be complied. Design rule check (DRC) and layout versus schematic (LVS) tools usage is necessary to verify layout correctness.

Post-layout simulation is the next step in the design flow after successful layout design. Most common one tool IC design approach typically assumes only quasi-static method of extraction of parasitic resistance of each net and the self-capacitance of each net to the ground. However, this approach becomes ineffective in case of high operating frequencies and increase of circuits complexity.

Two tool approach implements advanced EM simulation capabilities increasing simulation accuracy while shortening design time and also reducing human errors [4]. In NI AWR Design Environment based verification flow designer send MMIC layout from manufacturing tool to an EM simulation tools like AXIEM or Analyst to make sure the design works properly.

AXIEM planar method-of-moments (MoM) EM analysis tool is a frequency-domain solution that meshes only conductors and uses Green's functions to calculate the effect of conductor currents on each other. In MMIC design applications MoM solver is typically used for simulation of distributed lines connected by vias, where modeling phase delay is critical, for example, spiral inductors, interconnections between stages, power and ground buses.

Analyst 3D finite element method (FEM) EM simulation tool produce a volumetric mesh for solving for the electric fields using Maxwell's equations. It is effective for arbitrary volumetric structures such as wire-bond/bond pad interfaces, IC packages. However, this technique has high requirements to computing resources, which lead to increase of simulation time.

IC designers can use multiple EM techniques to compare the results from different simulators in order to determine which of the method the best for a given design is.

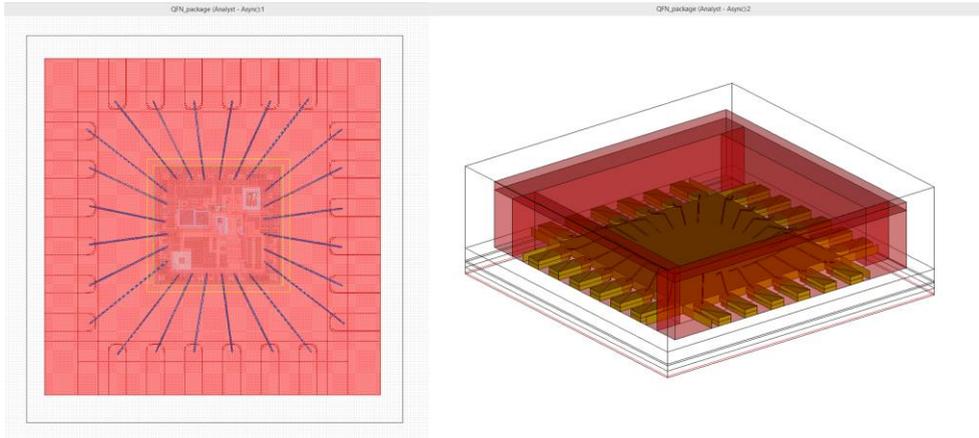


Fig. 3. Core Chip packaging EM simulation.

The coupling can be simulated by assigning 2N ports for N bond wires in Analyst tool. The cross-terms (S31, S13, S14 etc.) are the responsible for the accounting of coupling between the bond wires. The designed MMIC post-layout simulation test bench is shown in Fig. 4.

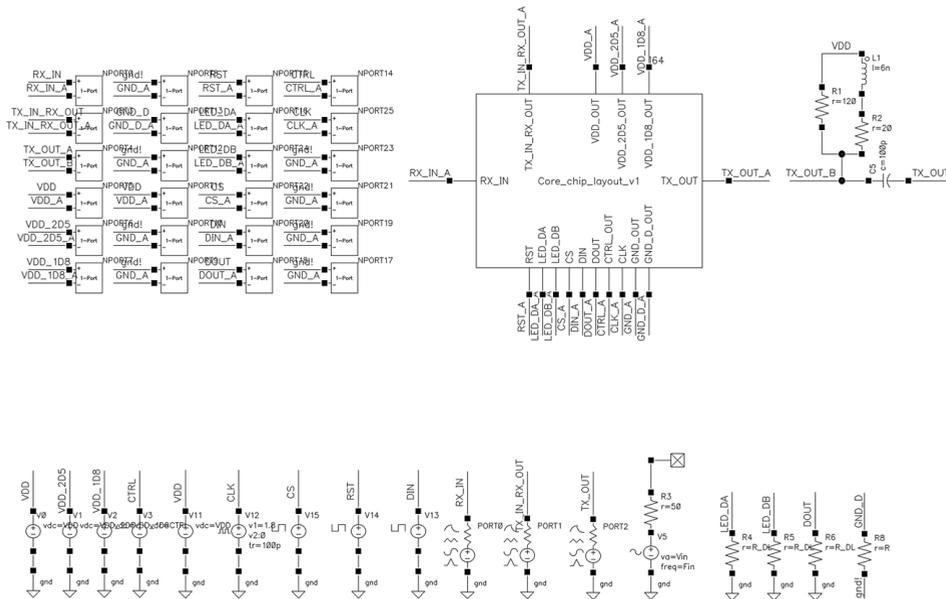


Fig. 4. Core Chip testbench.

The EM simulation results are taken into account by means of n-port components. They provide direct use of generated .s2p files or use other different netlist files obtained from the .s2p files by means of a non-linear broadband conversion [7].

3 Simulation results

The post-layout simulation results of the designed MMIC are shown in Fig. 5—10.

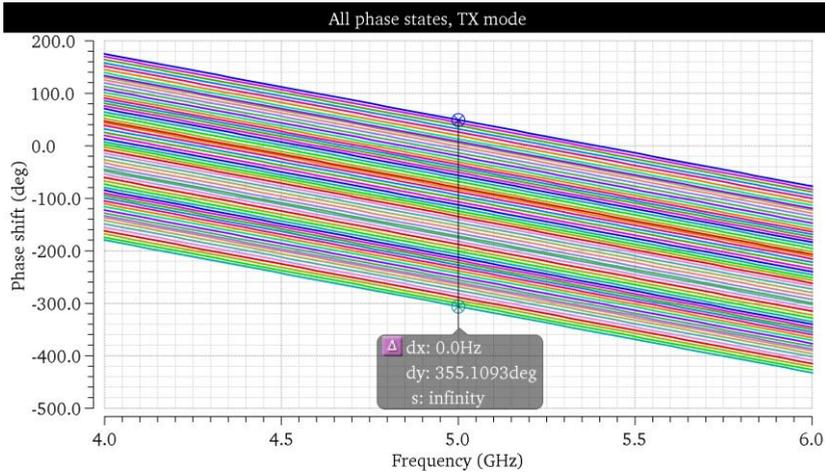


Fig. 5. Frequency dependence of the relative phase shifts from the control code in Tx mode.

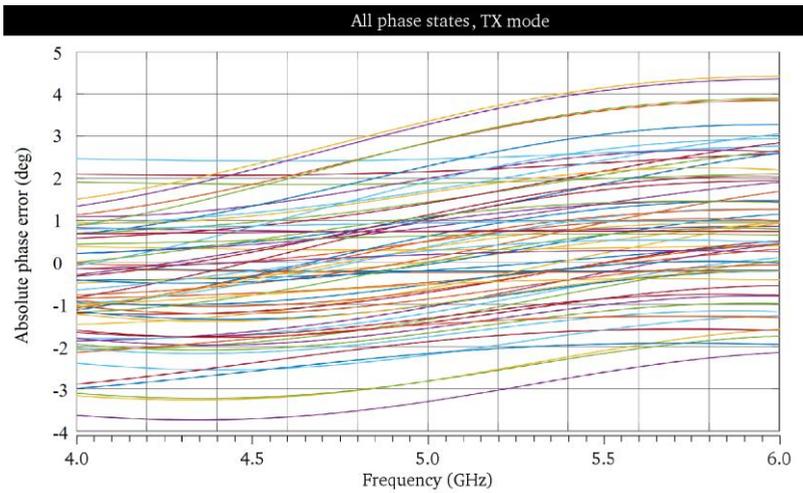


Fig. 6. Frequency dependence of the absolute phase error from the control code in Tx mode.

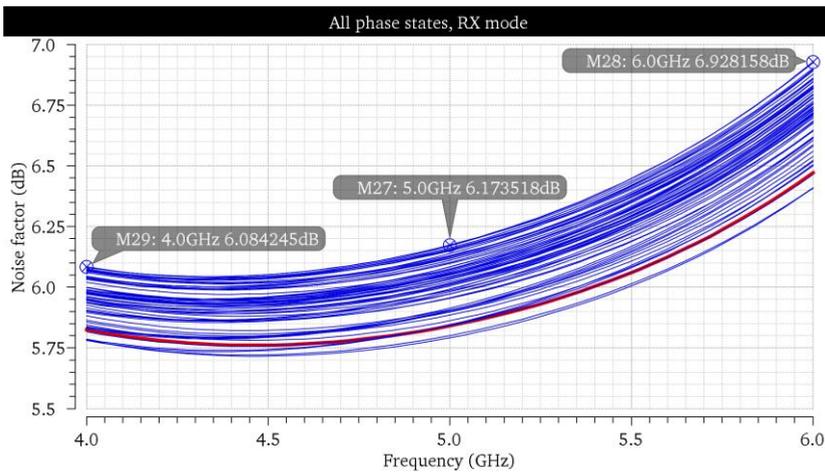


Fig. 7. Dependence of the noise figure in Rx mode from frequency.

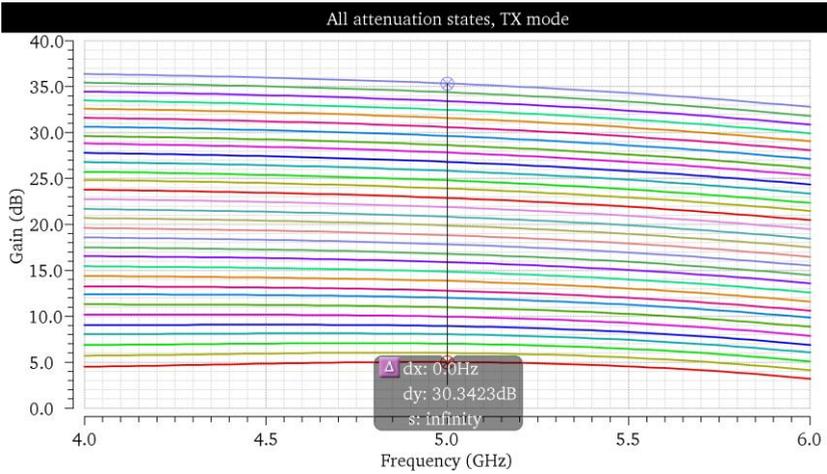


Fig. 8. Frequency dependence of the transfer ratio from the control code in Tx mode.

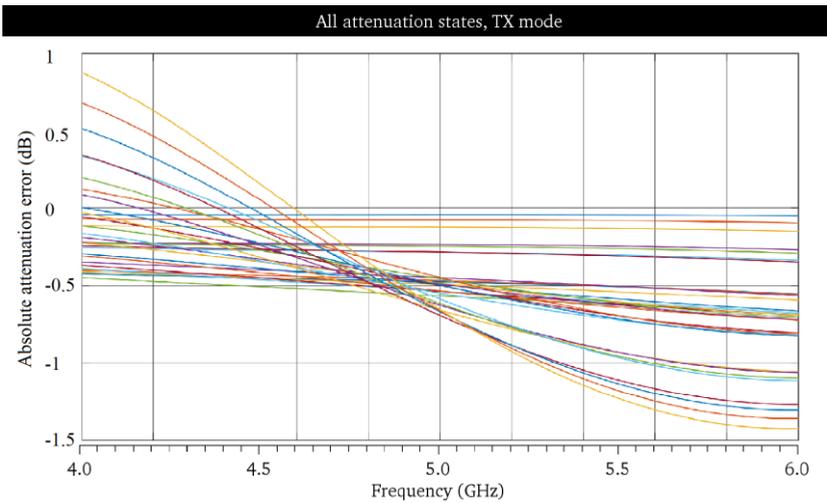


Fig. 9. Frequency dependence of the absolute attenuation error from the control code in Tx mode.

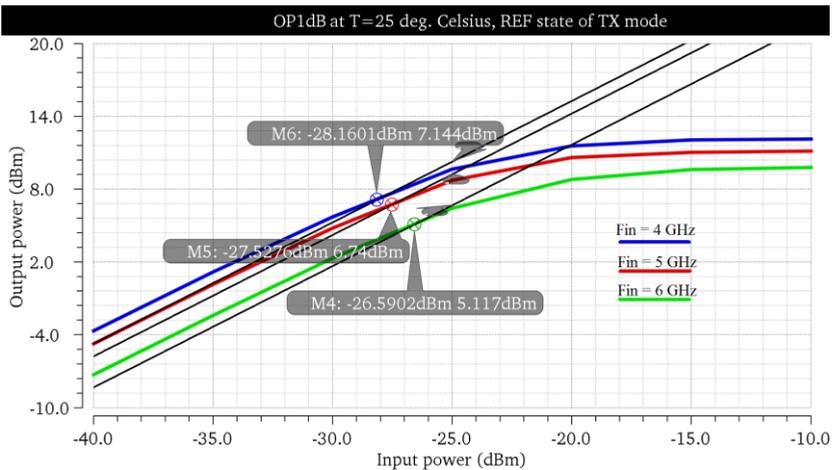


Fig. 10. Tx mode output 1 dB compression point simulation results.

Based on post-layout simulation results calculated root mean square (rms) values of the attenuation and phase errors in Rx mode do not exceed 0.2 dB and 1.5 degrees respectively. Similar parameters for Tx mode do not exceed 0.33 dB and 1.6 degrees.

Gain variation in the operating frequency range is below 1.9 dB in Rx and 3.5 dB in Tx modes respectively.

Noise figure of the MMIC in Rx mode is below 7 dB. Output 1 dB compression point in Tx mode is around 6.74 dBm at a 5 GHz.

The resulting post-layout simulation parameters of the Core Chip are shown in Table 1.

Table 1. Parameters of the designed Core Chip.

Parameter	Value, unit	Note
Operating frequency range	4–6 GHz	—
Operating temperature range	–60–85 °C	—
Gain	20.4/33	Rx/Tx mode
Gain variation	1.9/3.5	
Input return loss	12.1 dB	
Output return loss	10 dB	
Isolation between Rx/Tx channels	>50 dB	
Attenuation range	31 dB	
Attenuation step	1 dB	
Attenuation error	<0.33 dB	rms value
Phase adjustment range	360°	$f_{in} = 5$ GHz
Phase adjustment step	5.625°	
Phase error	<1.6°	rms value
Output 1 dB compression point	6.74 dBm	Tx mode, $f_{in} = 5$ GHz
Noise figure	<7 dB	Rx mode
Rx/Tx switching time	<15 ns	—
Tx/Rx switching time	<10 ns	—
Total power consumption	375/525 mW	Rx/Tx mode
Total layout area	6 mm ²	with pads

4 Conclusion

MMIC design flow features are discussed in the paper. Circuits yield optimization and precise post-layout simulation based on two-tool approach can increase the chances of successful ICs first tapeout and reduce its design cost. A key drawback of the presented design methodology is increased complexity of the post-layout simulation.

The concept of the C-band Core Chip design is presented. According to post-layout simulation rms attenuation and phase errors do not exceed 0.33 dB and 1.6 degrees. Total MMIC layout area is 6 mm². It was possible to exceed the characteristics of the known nearest analogues, which were developed earlier in Si-based processes. The use of parameters correction system ensures stability of the MMIC characteristics in a wide range of operating temperatures.

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