W-band voltage-controlled oscillator design in 130 nm SiGe BiCMOS technology

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Abstract. The paper presents design flow and simulation results of the W-band fundamental voltage-controlled oscillator in 0.13 µm SiGe BiCMOS technology for an automotive radar application. Oscillator provides fundamental oscillation range of 76.8 GHz to 81.2 GHz. According to simulation results phase noise is –89.3 dBc/Hz at 1 MHz offset, output power is –5.6 dBm and power consumption is 39 mW from 3.3 V source.

1 Introduction

In the present time Frequency-Modulated Continuous-Wave (FMCW) radars become more and more popular in autonomous vehicles and advanced driver-assistance systems. In W-band with 77 GHz carrier such radars provide greater operation range, distance resolution and robustness to the clutter in comparison with widely used ultrasonic sensors. One of the key functional blocks of the FMCW radar is a frequency synthesizer. It forms a signal with linear frequency modulation (also called chirp). Frequency synthesizers are usually made using phase-locked loop (PLL) in millimeter-wave. One of the main blocks in a PLL is a voltage-controlled oscillator (VCO), which generates single-tone signal whose frequency depends on a control voltage.

This paper presents schematic and simulation results of the integrated VCO with 77 to 81 GHz frequency range designed in 0.13 µm SiGe BiCMOS technology process with current-gain cutoff frequency/maximum oscillation frequency (f_T/f_{max}) of 300/500 GHz. Designed VCO is a part of W-band FMCW automotive radar MMIC.

2 Synthesizer structure

There are four main schemes of frequency synthesizers based on PLL in millimeter range: PLL with a fundamental VCO [1, 2], PLL with a push-push VCO [3], PLL with a frequency multiplier [4] and PLL with an injection-locked oscillator [5]. Comparison of these schemes is given in [6]. The author highlights several main differences of PLL-based frequency synthesizers that may limit their application in a particular implementation (such as level of phase noise, frequency range and output power).

First variant of synthesizer scheme is chosen for the designed radar MMIC. This scheme allows to obtain required frequency tuning range (4 GHz), level of phase noise and output power. Block diagram of the designed PLL-based frequency synthesizer is shown in Fig.1.

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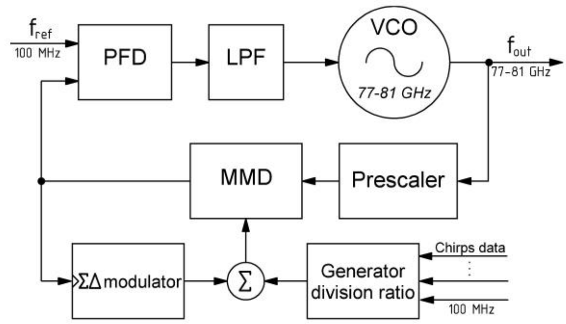

Fig. 1. Block diagram of the FMCW synthesizer.

In the presented frequency synthesizer designed VCO should provide oscillation frequency range from 77 to 81 GHz in temperature range from –60 to 85 °C with output power no less than –10 dBm.

3. VCO design

There are two main schemes of VCO in millimeter-wave: Colpitts VCO [1, 6] and cross-coupled VCO [7, 8]. Colpitts VCO was chosen for the design since it provides higher operating frequency, wider frequency range and lower phase noise in comparison with cross-coupled VCO [9]. Schematic of designed VCO is shown in Fig. 2.

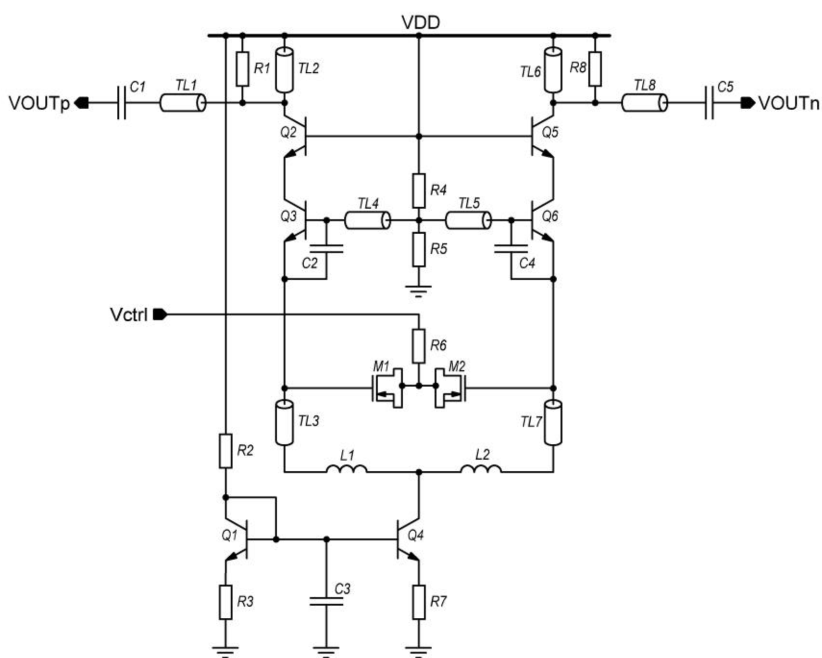

Fig. 2. Schematic of the W-band fundamental Colpitts VCO.

One of the most important oscillator characteristics is a phase noise (PN). Relative low gain of an active devices and unstable oscillations in millimeter range lead to the high PN. Main sources of PN are oscillatory circuit, bias circuits, current and voltage sources. There are several ways to reduce PN. It is necessary to use a symmetrical VCO scheme, provide high Q factor of the oscillatory circuit and high output power to achieve low phase noise [10]. In addition, to reduce PN the common-mode resistors R_4 and R_5 should be small (< 2 kΩ) but should not provide a short-circuit condition at common nodes to ensure differential-mode oscillation.

Voltage-controlled capacitance, usually built on varactors, is used to adjust the oscillation circuit. There are two ways to change oscillation frequency of presented scheme: by place varactors between base and emitter of Q3 and Q6 or by place varactors directly to the tank. Second approach is applied due to lower achievable PN in designed VCO.

Varactor is present in the used technology but its C_{max}/C_{min} is lower than required to obtain 4 GHz tuning range. To overcome this, transistors M1 and M2 are used instead varactor by the way shown in the Fig 2. Using MOS transistors as varactors allows to achieve higher Q factor in W-band since at the frequencies above 30 GHz Q factor of the varactor significantly decreases that strongly impact to the Q factor of the tank.

During design, there is a trade-off between Q factor of the tank and C_{max}/C_{min} of the variable capacitance (or frequency tuning range). Minimization of channel length of the MOS transistors using as varactors leads to an increase of Q factor but a decrease in the tuning range. In addition, increase in the gate number with constant total gate width allows to reduce gate resistance and increase in Q factor but decrease in C_{max}/C_{min} of variable capacitance because of parasitic capacitance.

The inductors are implemented using microstrip lines that made in a top-layer thick metal (TM1) and a bottom-layer (M1) used as ground plane. The tank inductance is approximately 45 pH ($TL_4 = TL_5 \approx 22.5$ pH). TL_2 and TL_6 are used as inductors at the VCO output to increase signal amplitude. Large spiral inductors L1 and L2 (150 pH) and decoupling capacitor C3 2 pF are added to block the noise coming from the tail current source, and to make impedance looking down to tail current source infinite [6].

4 Simulation results

Fig. 3 shows simulated oscillation frequency versus control voltage (V_{ctrl}) characteristic of the VCO at the different temperatures. VCO achieves oscillation frequency range of 76.8~81.2 GHz while control voltage varies from 0 V to 1.5 V at the normal conditions (27 °C). Required 4 GHz frequency range is located between 0.15 V and 1.22 V of control voltage.

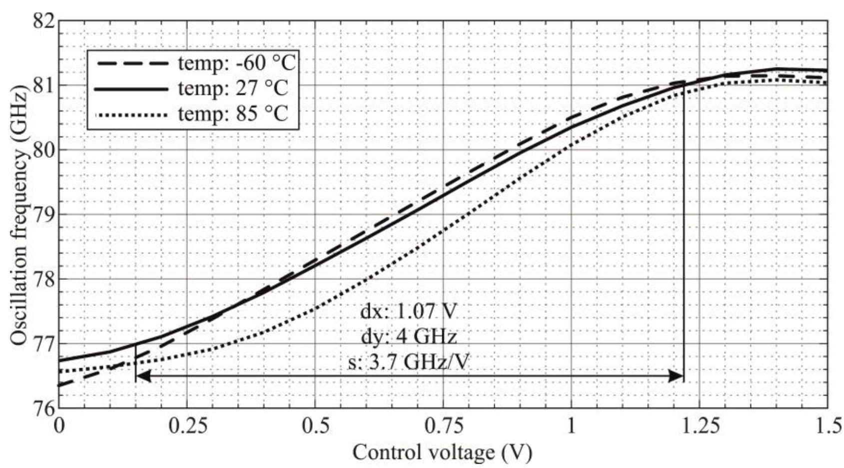

Fig. 3. Simulated oscillation frequency versus control voltage.

Fig. 4 shows dependence of oscillator output power at differences temperatures. Under normal conditions oscillator output power varies by 0.25 dBm in operating frequency band.

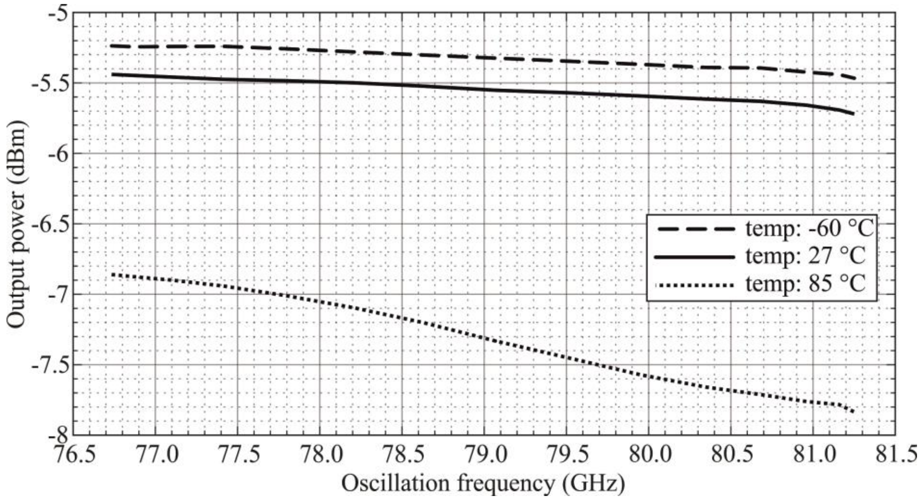

Fig. 4. Simulated output power versus oscillation frequency.

Fig. 5 shows the simulated phase noise at 1 MHz offset versus oscillation frequency characteristic of the VCO at 27 °C. Designed VCO achieves phase noise of –89.3~–90.2 dBc/Hz.

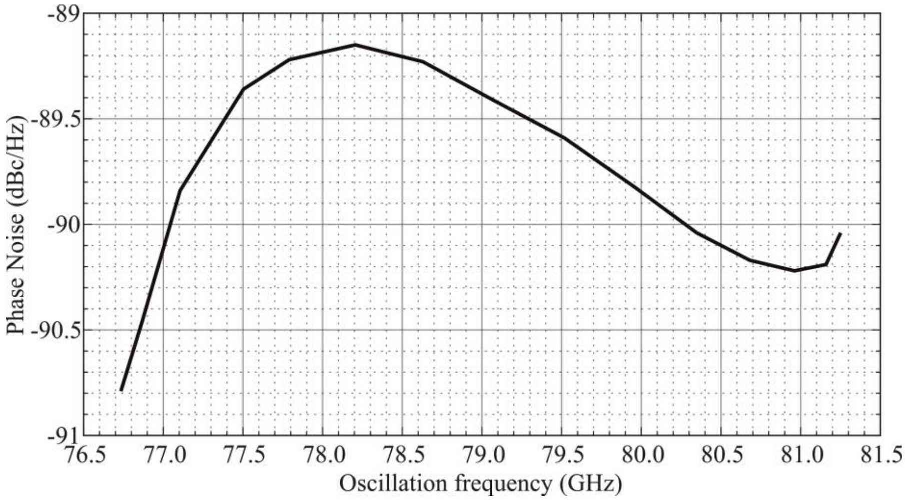

Fig. 5. Simulated phase noise versus oscillation frequency at 1 MHz offset.

The figure of merit (FOM) of the VCO that considers output power is defined as

$$FOM_2 = L\{f_{offset}\} - 20\log\left(\frac{f_0}{f_{offset}}\right) + 10\log\left(\frac{P_{DC}}{P_{out}}\right),$$

where $L\{f_{offset}\}$ is the phase noise in dBc/Hz at the offset frequency f_{offset} from the carrier frequency f_0. P_{DC} and P_{out} is the DC power dissipation and output power, respectively, both in mW.

Table 1 presents a summary of parameters of the designed W-band fundamental VCO schematic and recently reported state-of-the-art CMOS and BiCMOS VCO with similar operation frequency. Compared with other works, presented VCO exhibits low power consumption with relatively wide tuning frequency range.

Table 1. VCO performance summary and comparison.

Year [Reference]	**2014 [6]**	**2016 [1]**	**2018 [8]**	**2019 [This Work]***
Technology	0.13 µm SiGe CMOS	0.13 µm SiGe BiCMOS	90 nm SiGe BiCMOS	0.13 µm SiGe BiCMOS
Frequency range (GHz)	92.5-100.5	57-64	76.8-79.2	76.8-81.2
Control voltage (V)	0-2.5	0-2.5	0-1.0	0-1.5
Phase Noise @ 1 MHz (dBc/Hz)	–102	–90	–77.9	–89.3
FOM_2 (dBc/Hz)	—	–190.3	—	–171.1
Operating temperature range (°C)	—	—	—	–60-85
Power Consumption (mW)	90	72.6	49.6	39
Supply Voltage (V)	3.3	3.3	3.3	3.3
Area (mm^2)	0.05	0.12	0.21	~0.12

*Schematic simulation results

5 Conclusion

Schematic and simulation results of fundamental VCO with 77-81 GHz frequency range in 0.13 µm SiGe BiCMOS technology is presented. Tuning slope of designed oscillator is about 3.7 GHz/V. Phase noise is –89.3 dBc/Hz at 1 MHz offset. Oscillator consumes 39 mW from 3.3 V source. Designed VCO will be used in the radar MMIC after designing of layout and carrying out post-layout simulation.

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