Design of clock and data recovery system's behavioral model for high speed transceivers of serial interfaces

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Abstract. This paper provides a parameterizable behavioral model of a clock and data recovery system (CDR) based on phase-locked loop (PLL) for the receiver part of a high-speed serial interfaces. The model was used to calculate parameters and characteristics of the system as well as estimate their calculation error depending on the sub-circuit characteristics taken into account. A model structure was selected based on the obtained jitter estimation error. The model complies with all the accuracy and speed requirements to calculations of the characteristics of a PLL-CDR system for a receiver block with data transmission bit rates above 3.125 Gbit/s.

1 Introduction

The system of Clock and Data Recovery (CDR) is an integral part of high-speed transceivers of serial interfaces. A CDR system based on a PLL (phase-locked loop) circuit with a "bang-bang" phase detector [1] is a common type of CDR system architecture [2].

High-level behavioral models have gained widespread use at the stage of PLL-CDR system characterization. A behavioral model uses parameters of certain sub-circuits of the transistor model, which enables highly accurate calculations at the stage of behavioral modelling of the system. Behavioral models used at schematic design step have the following advantages:

– unlike analytical methods [3–5], modelling allows describing not only the steady-state operating mode of the system, but also the initial transition process.

– simulation of a behavioral model is several times faster than simulation of the electric circuits, their components being represented by physical models of BSIMv4 type (the reference model).

However, behavioral models require, firstly, estimation of the calculation error because they do not take into account all the characteristics of electric circuits of the reference model; and secondly, determination of a set of parameters to take into account to achieve an acceptable calculation error. The value of error depends on the relation between deterministic jitter J_D of the receiver clock signal and the value of bit interval *UI*. The calculation for the transceiver reference model shows that the value of J_D for the speed of 3.125 Gbit/s is ~8 ps at *UI* = 320 ps. As far as $J_D << UI$, the relative error of determinate

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jitter calculation (relative to the reference model) of $\delta J_D < 50\%$ is acceptable for this purpose.

The paper estimates the error of parameters calculation performed using the PLL-CDR behavioral model and the influence of sub-circuit parameters and characteristics on the error. To check the results, a behavioral model of PLL-CDR system for a receiver with the bit rate of 3.125 Gbit/s was developed using Verilog-AMS hardware description language followed by a comparison with the reference model.

2 Main parameters and characteristics of the system

The following parameters and characteristics describe the transition process of frequency $F_{RX}(t)$ and phase $\varphi_{RX}(t)$ of the receiver clock signal being recovered :

1. Transition time τ_{CDR} to locked state;
2. Maximum allowed initial relative frequency difference:

$$\delta F_{max}(0) = [F_{BIT}(0) - N \cdot F_{RX}(0)]/ F_{RX}(0) \cdot 100\ [\%] \quad (1)$$

where F_{BIT} is input data bit rate, and N – initial step bit frequency step-down ratio (depends on the receiver architecture);

3. Deterministic jitter:

$$J_D = \Delta\varphi_{RX}{}^{max} / (2\pi \cdot \langle F_{RX} \rangle \cdot UI)\ [\text{UI}] \quad (2)$$

where $UI = (2 \cdot \langle F_{BIT} \rangle)^{-1}$, $\langle F_{RX} \rangle$ and $\langle F_{BIT} \rangle$ – average values of the corresponding parameters, and $\Delta\varphi_{RX}{}^{max}$ – the amplitude of oscillations $\varphi_{RX}(t)$ measured in the locked state.

4. $JTF(f_{Jin})$ jitter transfer function – the ratio between output jitter amplitude A_{Jout} and input jitter amplitude A_{Jin} depending on the frequency of change A_{Jin}.

5. $KJ(A_{Jin})$ determinate jitter transfer ratio – the ratio between output jitter amplitude A_{Jout} and input determinate jitter amplitude A_{Jin}.

3 Sub-circuits of the system and their parameters

Figure 1 shows an overview diagram of PLL-CDR. Each of the sub-circuits and its models are described below.

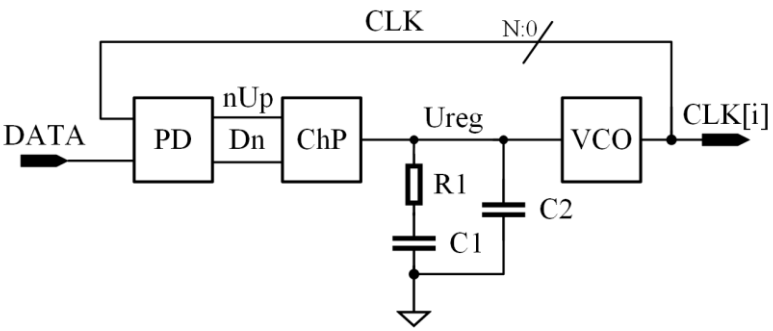

Fig. 1. PLL-CDR architecture.

The phase detector (PD) used in the work is a modified version of a classic bang-bang phase detector. The circuit generates digital voltage pulses *nUp* and *Dn* at the positive and negative phase difference $\Delta\varphi(t)$ between the clock signal and the data signal, respectively. The main parameters of this block are delay τ_{PD} as well as the set T_S^{rise}, T_S^{fall} and hold T_H^{rise},

T_H^{fall} times of the input flip-flops. Accordingly, two behavioral models represent the block: including these parameters (PD_{SH}) or excluding them (PD_F).

The charge pump (ChP) block transforms signals *nUp* and *Dn* into the charge and discharge current of the lowpass filter. The main parameters of it are charge current I_P, discharge current I_N, current mismatch $\Delta I = (I_P - I_N)/(I_P + I_N)$ and the dependency of these currents from the output voltage $I_P(U_{REG})$, $I_N(U_{REG})$. Therefore, the paper presents three models of ChP: with balanced currents (ChP_F), with account of current mismatch (ChP_{UC}) and with account of the dependency from the operation point (ChP_{OP}). PLL-CDR uses lowpass second-order filter.

The voltage-controlled oscillator (VCO) is characterized by voltage-frequency characteristic K_{VCO}. The paper proposes two behavioral models of the voltage-controlled oscillator: linear voltage-frequency characteristic with the sloping calculated for (VCO_{LN}) operating point and a voltage-frequency characteristic taking into account the operating point (VCO_{NLN}).

The equivalent feedback circuit delay τ_{LB} determines the total delay in all sub-circuits in the PD – ChP – VCO path.

Table 1 lists the general information about the sub-circuit models described above.

Table 1. The list of sub-circuit models.

#	Name of sub-circuit model	Description
1	PD_F	Functional model
2	PD_{SH}	Model with account of set T_S^{rise}, T_S^{fall} and hold T_H^{rise}, T_H^{fall} times of input flip-flops
3	ChP_F	Model with balanced currents I_P, I_N
4	ChP_{UC}	Model with account of current mismatch ΔI
5	ChP_{OP}	Model with account of the dependency from the operating point
6	VCO_{LN}	Model with the linear voltage-frequency characteristic
7	VCO_{NLN}	Model with the non-linear voltage-frequency characteristic

4 Error estimation of the behavioral model

The procedure of error estimation for each of the parameters of the sub-circuits listed in table 1 is as follows :

1. The sub-circuit of the reference model is substituted by its behavioral model.
2. The parameters of this model are calculated and compared to those of the reference model.
3. The procedure is repeated for a more complex sub-circuit model.

Table 2 shows the results of PLL-CDR system modelling in the time domain consisting of sub-circuit combinations described above and relative errors with respect to the reference model for each of the parameters. The modelling conditions: K.28.5 sequence of 8B/10B code. As far as the time required for determining parameter $\delta F_{max}(0)$ is comparable to that of the reference model calculation even when one of the sub-circuits is substituted by a behavioral model, the calculation was performed using only the behavioral model consisting of the models with the least error of parameter J_D.

The maximum J_D error reduction takes into account the dependency of the output ChP current from the operational point.

Table 2. Comparison of simulation results.

Block	Model type	Parameter			Relative error with respect to the reference model for the parameter: $(P_{ref} - P_{beh})/P_{ref}$, %			Simulation time, min
		τ_{CDR}, ns	$\delta F_{max}(0)$, %	J_D, UI	τ_{CDR}	$\delta F_{max}(0)$	J_D	
Reference model		150	0.54	0.0243	—	—	—	149.36
PD	PD_F	110	—	0.0231	27	—	4.9	—
	PD_{SH}	123	—	0.0249	18	—	2.5	—
ChP	ChP_F	294	—	0.0186	96	—	23.5	—
	ChP_{UC}	387	—	0.0269	158	—	10.7	—
	ChP_{OP}	204	—	0.0245	36	—	0.8	—
VCO	VCO_{LN}	86	—	0.0281	43		15.6	—
	VCO_{NLN}	113	—	0.0257	25		5.8	—
PD_{SH} + ChP_{OP} + VCO_{NLN}		127	0.66	0.0244	15	18	0.4	0.25

Figure 2 shows the influence of value τ_{LB} on value J_D. The dependency has non-linear nature and disrupts the relation $\delta J_D < 50\%$ only when the value τ_{LB} is more than 3.4 times different from that for the reference model.

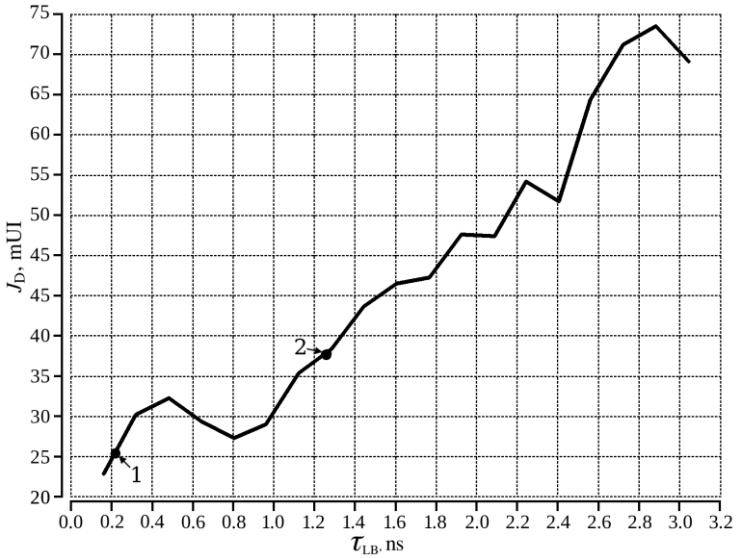

Fig. 2. The dependency of J_D on τ_{LB} value: 1 – the point corresponding to τ_{LB} for the reference model; 2 – the point where the deviation of J_D value from the reference value exceeds 50%.

Figure 3 shows characteristic $JTF(f_{Jin})$ calculated using the reference model and a set of PD_{SH} + ChP_{OP} + VCO_{NLN}. The conditions: pseudorandom code PRBS31 with sinusoidal jitter with the amplitude of 0.1UI and frequency varying in the range of 1 ÷ 1000 MHz. The error of the model across the whole range does not exceed 31 % (in 60 MHz point).

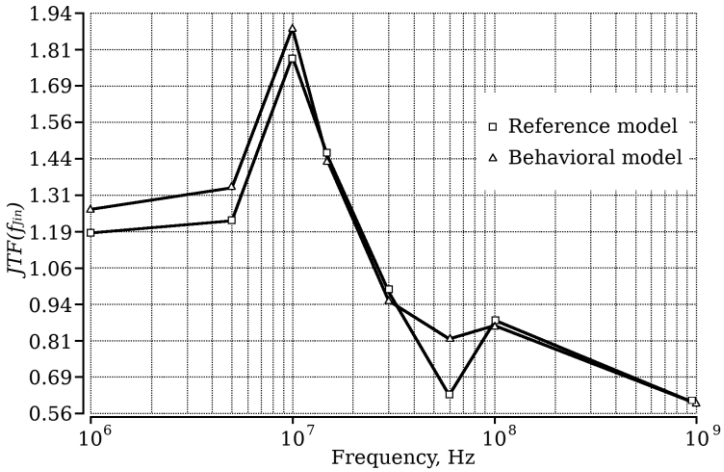

Fig. 3. Characteristic $JTF(f_{Jin})$ calculated using the reference (a square marker) and behavioral (a triangular marker) models.

A similar comparison has been performed for characteristic $KJ(A_{Jin})$. Figure 4 shows the corresponding dependency. The conditions: input code K.28.5 of 8B/10B code with deterministic jitter. The value of the input jitter varies in the range from 0.1 UI to 0.5 UI. The error of the model across the whole range does not exceed 36 % (in 0.1 UI point).

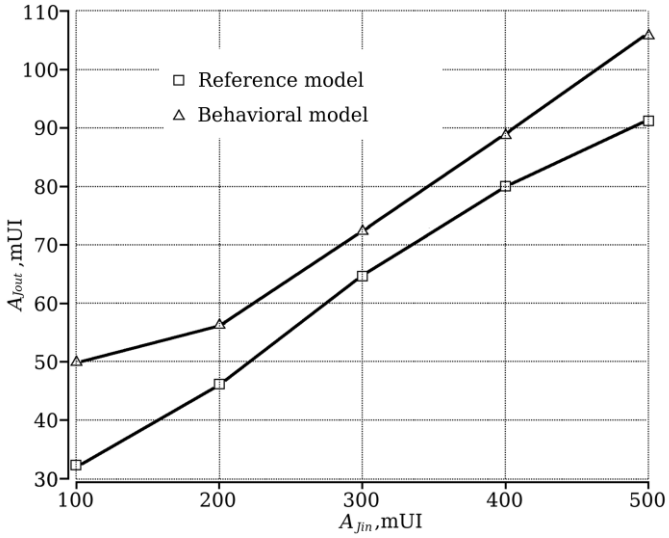

Fig. 4. The dependency of output jitter amplitude A_{Jout} of the clock signal on the input jitter amplitude A_{Jin} calculated using the reference (a square marker) and the behavioral (a triangular marker) models.

The calculations show that the developed model consisting of PD_{SH} + ChP_{OP} + VCO_{NLN} meets the requirement of δJ_D < 50% and is suitable for PLL-CDR system parameter estimation.

5 Conclusion

Different options for behavioral models of PLL-CDR sub-circuits were studied. The error of behavioral models of sub-circuits was analysed in comparison with the reference BSIMv4 type model depending on the sub-circuit parameters.

A parametrizable behavioral model of PLL-CDR system complying with the error requirement was developed using Verilog-AMS hardware description language. The value of deterministic jitter J_D obtained using the behavioral model is 8.1 ps, and that obtained using the reference model is 7.8 ps. Therefore, the relative error of determinate jitter δJ_D calculation is less than 4%.

The error of $KJ(A_{JD})$, $JTF(f_{Jin})$ calculation does not exceed 36%. The developed model allows calculating the transition process of PLL-CDR system ~10^3 times as fast as the reference model and calculating BER using method [6]. The developed model can be used to calculate PLL-CDR characteristics with arbitrary bit rate.

References

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