

Experimental study silicon low-dimensional structures for generation of THz radiation

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Abstract. Capabilities of precision technologies for manufacturing on SOI wafers of silicon low-dimensional structures for terahertz generation are investigated. The design of diode device based on array of silicon nanowires or on ultrathin (<10 nm) silicon layer are proposed. This generating silicon diode includes nano-sized elements with ballistic transport of carriers, which is coupled to a metal antenna made from silicide layer.

1 Introduction

Silicon one-dimensional structures are promising for use in various nanoelectronic devices - in nanoscale field-effect transistors, photonics structures, and quantum computing. The use of nanowire structures was also investigated for biosensor applications, which make it possible to achieve sensitivity to single adsorbed atoms and molecules [1]. In this study, the development of technologies for the formation of an array of silicon nanowires is part of the work on the creation of THz range receivers and sources based on their early theoretical studies.

Potentially, anisotropic plasma-chemical etching allows the formation of silicon structures with critical sizes up to 10 nm, but the defects created by ion bombardment lead to a significant decrease in the electron mobility in the formed one-dimensional silicon structures (nanowires).

To reduce the phenomenon of mobility degradation, a four-step process has been proposed: 1) high-resolution electron beam lithography followed by heat treatment of negative HSQ resist, 2) highly anisotropic and selective plasma etching of silicon with an accuracy of lithographic transfer of 1 nm, 3) precise thermal oxidation of nanowire structures, and 4) selective removal of the thermally oxidized defective surface layer by liquid etching in an HF buffer.

We used SOI (100) orientation wafers with a p-Si (50 nm) / SiO₂ (200 nm) / Si substrate structure.

To obtain an NW-Si array with a cross-section size of up to 10 nm, electron lithography and anisotropic plasma-chemical etching were used. An important element of the technology is controlled oxidation of the Si surface by the RTP method followed by selective liquid etching of SiO₂ to remove the defective silicon layer and further reduce the transverse dimensions of the nanowires.

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The output of terahertz oscillations generated in a low-dimensional BARITT diode is assumed through a planar spiral antenna made in a silicon layer of NiSi metal silicide. The contacts to it were fabricated by ultrafine high-dose doping of the Si contact areas with plasma-immersion ion implantation of boron, while the nanowires themselves remained unalloyed or lightly doped.

To diminish the possible effect of the silicon substrate on the generation of THz vibrations in the nanowire structure, direct measurements of the transmission of terahertz radiation (0.25–2.5 THz) through the SOI plate were performed, and its insignificant (less than 3 cm^{-1}) absorption in volume of lightly doped silicon substrate.

2 Process of structure formation

Structures were formed using electronic lithography. Negative electronic resist HSQ XR-1541 has good plasma resistance and mechanical stability.

Samples were prepared on SOI plates (50 nm Si / 200 nm SiO₂), 2×2 cm in size. A 6% HSQ solution was used for deposition, the initial resist layer thickness was 50 nm. The lithography was carried out on a Raith 150 EBL system at an electron energy of 30 keV. This process was optimized to create a mask with a critical size of up to 10 nm by an electron beam of ~ 1 nm. The developed mask structures were annealed in the atmosphere for 30–60 minutes at 400 °C. Fig. 1 shows a cross section and a top view of a resist mask.

Plasma etching of silicon was carried out in a PlasmaLab 100 tool (Oxford Instruments Plasma Technology, UK) in a mixture of SF₆ and C₄F₈. By changing the ratio of SF₆ to C₄F₈, angle of the side wall profile can be adjusted. Increasing the ratio improves the etching rate, but decreases selectivity and decreases the profile angle. An increase in plasma power again reduces selectivity with a slight improvement in etching rate. The composition of the gas mixture was optimized in a separate experiment to obtain a vertical profile of the side walls of the Fin structures, and was 5:9 (SF₆:C₄F₈). Other control parameters are as follows: pressure P=10–15 mTorr, discharge power W = 1200 W and RF bias power W_{RF}=30 W (equivalent to a constant bias potential of 170 V). The plate temperature stabilized at 20°C. As a result, the developed process allows one to achieve the selectivity of silicon etching to the XR-1541 resist up to 14:1 [4], the lithographic size leaving less than 1 nm.

The control of profile slope, critical size deviation, and aspect-dependent effect (ARDE) etching were investigated on test structures on standard silicon substrates. The ARDE effect becomes noticeable when the nanowires in the array are closer than 200 nm. As a result of optimization, the achieved parameters were as follows: vertical profile 90 ± 0.5 degrees, anisotropic etching rate of Si is about 300 nm / min.

The etching technology was then transferred to SOI wafers. Due to the charging of the underlying dielectric layer from the plasma, an increase in the RF bias voltage by 10% was required. In the case of an SOI wafer, silicon oxide is a stop layer for the etching process, and therefore.

The process of precision oxidation of the surface of nanowire structures was carried out in an AnnealSys AS-one tool with a controlled flow of dry oxygen and water vapor. The oxidation rate was accurately calibrated by ex situ ellipsometry, measured on the surface of the samples of silicon wafer witnesses. Subsequent removal of silicon oxide from nanowire structures in a 5% buffer solution of hydrofluoric acid made it possible to obtain “suspended” silicon nanoconductors. This approach allowed a controlled decrease in the cross section of nanowires by 2–6 nm with an increase in the mobility of carriers in Si nanowires.

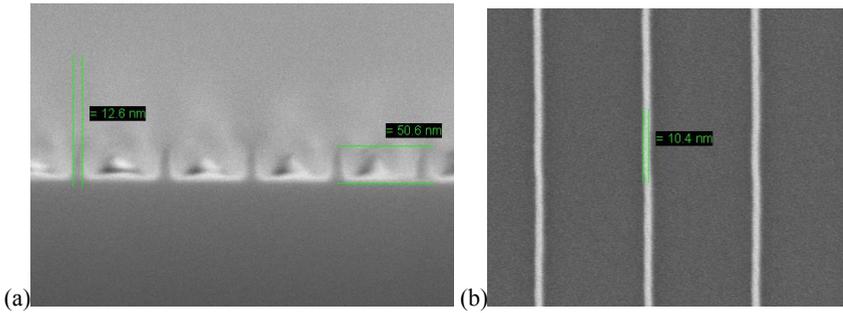


Fig. 1. (a) Cross-sectional SEM of HSQ 12 nm lines with 120 nm spaces in exposed 50 nm thick resist at 30 keV. (b) top view image.

The cross section of the initial test structures on bulk silicon is shown in Fig. 2. Fin structures up to ~ 10 nm wide with an aspect ratio of up to 10: 1 were obtained. The results of plasma etching of structures on SOI wafers and subsequent oxidation of nanowires are shown in Fig. 3a. When the surface of nanowires is oxidized, a visible increase in the cross section of structures occurs. Unfortunately, there is no possibility of observing the cross section of Si nanowires in a suspended state, but they can be observed in a plan view (Fig. 3b).

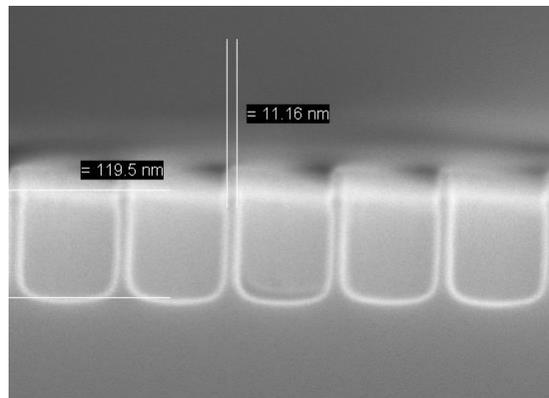


Fig. 2. Cross-sectional SEM of 11 nm Silicon fins with the remaining resist after RIE.

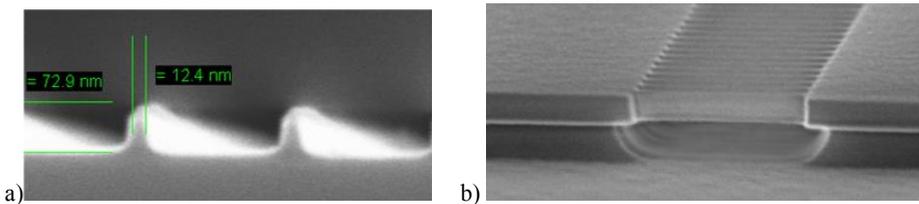


Fig. 3. a) Cross-sectional SEM Silicon fins on SOI samples after oxidation with 12 nm width, b) Released from SOI-substrate nanowires (18 nm) after wet etch.

3 Simulation of Defects profile

In order to determine density distribution of defects in Silicon we have to take into consideration the interaction of the energetic particles from plasma with the fin structure during processing. The remaining SiO_x lithography mask (in our process not less than 20 nm) preserves the top surface of fin from plasma particles bombardment, so the flow of

particles on the sidewalls plays the main role. The etch rate were assumed constant, so the top part of sidewall is more susceptible to the producing of defects from plasma exposure. The main reason for sidewall bombardment is the scattering of ions accelerated in a sheath near plasma-surface boundary on neutral molecules even at low pressures. The angular distribution of scattered particles and the loss of their energy were determined by the Monte Carlo code using TRIM gas approach [5] taking into account the pressure and the Langmuir sheath width. The latter was estimated from electron temperature, and concentration of ions in the plasma, measured under similar conditions using the Langmuir probe technique adapted for depositing plasma measurement [6].

Approach developed earlier [7] for modeling the distribution of dopants in fin-structure provided by plasma immersion ion implantation at elevated gas pressures. The projected range (R_p), the standard deviation in direction of projectile (ΔR_p) and radial straggling (ΔR_s) of recoils in silicon in wide range of energies was determined by TRIM [5]. Then the Monte Carlo procedure was again used, using the angular and energy distribution of the ions passing through the plasma layer as the initial input data at the Silicon surface. For each value of the angle and energy, using the (R_p), (ΔR_p) and (ΔR_s) values, the profile of the distribution of recoil atoms was calculated. The recoils in Silicon oxide (BOX and mask regions) were neglected as well as defects migration from surface to deeper layer during annealing.

The calculation was carried out on a grid of 0.5 by 0.5 nm. The calculated defect profiles for different fin aspect ratio parameter are presented in Figure 4 (a, b, c); it can be seen that the concentration of defects decreases logarithmically with the depth from the side surface of the structure. More than 0.999 parts of defects are concentrated in the surface layer with a width of about 3 nm. Oxidation of this layer removes those defects.

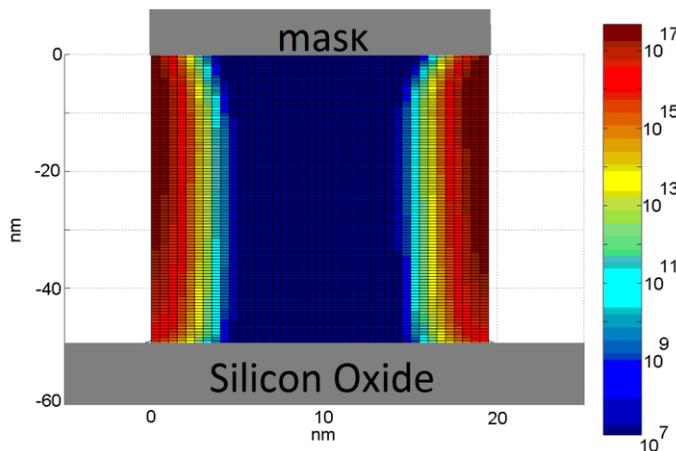


Fig. 4. Silicon recoil concentration (cm^{-3}) in the 50 nm height fin structure.

4 Results of electric measurements

To estimate influence of the defect layer on silicon surface after plasma etching the current-voltage characteristics of fabricated structures of silicon nanowire arrays were measured before and after removal of damaged layer. The static I-V curve were obtained on Si-NW array samples by using Keithley 4200-SCS with probe station. Gate voltage in the range of 0 - 5 V was also applied to substrate during measurements (Fig. 5, the regime of back-gated pseudo-FET). Observed drastic difference in current density between samples just after plasma etching and same samples with removed damaged layer is of 6 orders of magnitude. After plasma etching the current density through Si-NW is about $3 \cdot 10^{-5} \text{ A/cm}^2$ @ 1 V, and

after removal of damaged layer is $54 \text{ A/cm}^2 @ 1 \text{ V}$, $V_G = 0$. This effect solely attributed to dramatic decreasing of carriers scattering on defects on surface damaged layers.

Since the oxidation rate of defected layer was well controlled, that experiment allows us to estimate the thickness of Silicon surface layer reducing conductivity so much. In the case under consideration, it turned out to be about 3–4 nm. This is consistent with results of TRIM modelling of defects profile caused by ion bombardment of sidewalls of Si-fins during plasma etch process.

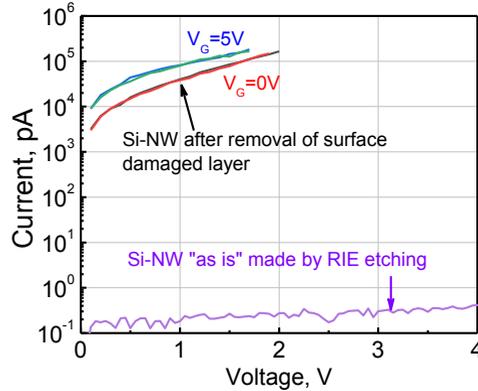


Fig. 5. IV curve for sub-10 nm suspended Si-NW array on SOI after RIE and after removal of damaged surface layer.

5 Conclusion

The application of the technology of accurate plasma etching and subsequent oxidation on SOI wafers allowed us to form a key element of the diode structure for THz generation — arrays of nanowires with a cross section of 10–20 nm and a length of 200 nm and higher. Controlled silicon oxidation removes the damaged layer and transfers the array of NW-Si nanowires on the surface to a suspended state (suspended NWs), in order to obtain the necessary conditions for ballistic span of carriers in the structure of the generating diode.

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