Design of High-Power High-Efficiency Broadband GaN HEMT Power Amplifier for S Band Applications using Load-Pull Technique

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Abstract. This work reveals the design for broadband high-power high-efficiency GaN HEMT power amplifier, operating in the frequency band ranging from 2.15 GHz to 2.65 GHz. The proposed structure is implemented using Cree GaN HEMT CGH40010 transistor. The high-power and high-efficiency performances over the broadband bandwidth are achieved using the load-pull technique. The proposed power amplifier is unconditionally stable over the entire operating frequency band. With the neatly designed matching circuits, the introduced power amplifier shows an excellent input/output matching. The simulated results show a flat power gain of 15 dB with an output 1-dB compression point of 14 dB. In terms of large-signal performance, the proposed amplifier reaches a saturated output power of 41.3 dBm (~13.6 Watts) with a PAE of 64% and a drain efficiency of 72%. The proposed design achieves an excellent linearity with an output third order two-tone intercept point TOI of 48 dBm.

1 Introduction

A power amplifier (PA) is usually located just before the antenna, and drives the transmitting power of the communication system [1-3]. It is the final amplification stage before the transmission of the RF signal, and as a result, it must provide enough output power to overcome channel losses between the transmitter and the receiver [4-5]. In a transmitter, the PA is the primary consumer of power; therefore, a major design constraint is how efficiently the PA can convert DC power into RF power [6-8]. The efficiency it can be translated either as longer battery life for example in case of wireless handheld or as lower operation cost, for example in case of cellular base station [9-11]. Another key requirement in today's microwave and radio frequency (RF) PA is the linearity; the PA input/output relationship must be linear in order to preserve the RF signal integrity [12-15]. However, the PA design often involves the trade-off of linearity and efficiency.

Referring to PA design, the output matching network that is always designed to deliver the maximum possible power, must be at the same time low loss to reaches the maximum possible PAE. In terms of PA design sequence, the output matching is designed first and the input matching is synthesised last [16-18].

Various techniques can be used to precisely determine an active device's input/output impedances at large-signal conditions, a crucial requirement for successful PA circuitry design. Among such techniques, the source-pull and load-pull techniques, which are used to determine source and load conditions for an RF active device that allow achieving an optimum solution in terms of PAE, output power, IP3 and ACPR [19-21].

In this paper, a high power high efficiency broadband GaN power amplifier operating in the frequency ranges from 2.15 GHz to 2.65 GHz is resented.

The paper is organized as follows. In section 2, the PA design flow is presented and described. Section 3 is devoted for the obtained results and discussions, while the concluding remarks are summarized in section 4.

2 The proposed PA design flow

2.1 Overview

The design of a PAs for a specific frequency range and application is a complex task in the sense that they have to fulfil several requirements, which are in many cases tradeoffs.

On the other hand, the PA performance requirements in terms of operating frequency band, output power, gain, noise figure, linearity, PAE, stability, input/output VSWR etc. are determined by the design process, active device technology/type, matching networks, biasing schemes, the operating class, the number of gain stages and the circuit size and topology.

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However, regardless of its target application, and up to the designer, the PA design may grouped into the following steps:

1. Design specifications
2. The Active device type/technology selection
3. DC analysis
4. Stability analysis
5. Biasing Networks design
6. Matching networks analysis/design
7. Circuit analysis and optimization

In this work, starting from the design specifications, the first pass resides in determining the design process and the subsequent selection of the active device. The latter is selected according the design specification goals in terms of the operating frequency band, output power, IP3 and PAE. After the proper active device selection, the subsequent step resides in DC analysis. The latter aims is to determine the proper biasing point according to the targeted operation class.

On the other hand, the stability analysis is an important part in the design process. The proposed PA is to be designed for an unconditionally stability over the entire operating frequency band. The easy way to achieve unconditionally stability is by using series resistors at the active device input/output. However, in case of PA design, a special care should be taken during the stability components selection/places to avoid any degradation of the gain and output power performances.

Whereas, the remaining steps consist of the biasing and matching networks design as well as the circuit analysis and validation. Basing on the DC analysis results, the biasing circuits are designed using microstrip line while the matching networks are synthesised using the load-pull technique.

In this work, the proposed matching networks are designed to provide the required bandwidth with an appropriate guard band. With the aim to reduce the size, the biasing networks are incorporated as part of the matching networks.

2.2 DC analysis and Q-point selection

According to the design specifications, the adopted active device in this work is CREE CGH40010. The latter is an unmatched, gallium nitride (GaN) high electron mobility transistor (HEMT). It operates from DC up to 6 GHz. The DC I-V characteristics curves of the used active device are illustarted in figure 1.

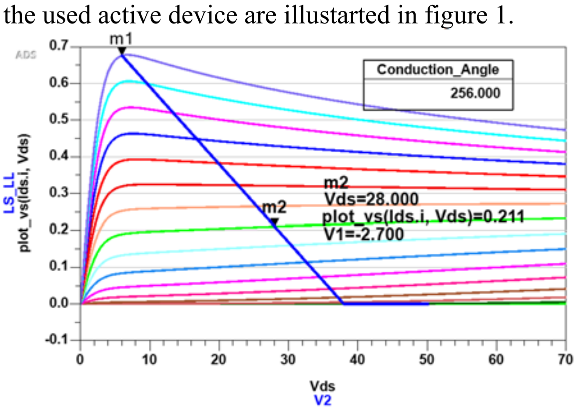

Fig. 1. DC I-V characteristics of the adopted active device.

With the aim to gain good linearity as well as high efficiency while balancing with the other design specification requirements, the proposed PA is designed to operate in class AB. In such class, the amplifier have no DC power consumption in the absence of the RF input (which is an advantage) and the drain current I_{ds} flows for a conduction angle between π and 2π.

As we can remark from figure 1, the proposed PA is biased around the class AB, and the selected biasing point is: $\{V_{ds} = 28v; V_{gs} = -2.7v\}$.

2.3 Stability analysis

By default, the adopted active device is not stable over its entire operating frequency ranging from DC to 6 GHz. As a result, a stabilization action is needed in order to achieve the unconditionally stability. The proposed stability circuit is illustrated in figure 2. Here, the emplacement of the stability series resistor is very important, it should be placed before the active device to avoid any degradation of de gain and output power. In addition, the selected stability resistor value represents the best value that combines the unconditionally stability with a good gain.

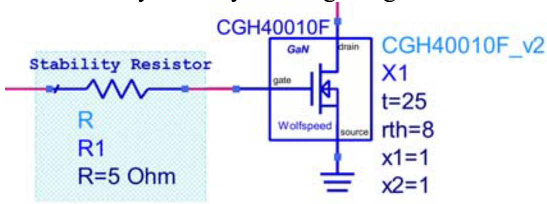

Fig. 2. The proposed stability network

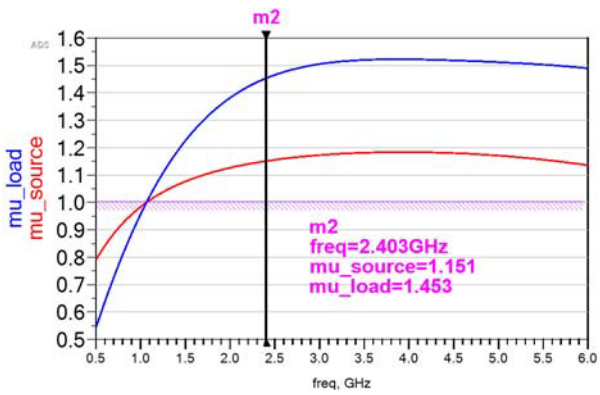

Fig. 3. Stability analysis results using Edwards-Sinsky stability factors μ and μ prime.

On the other hand, the stability analysis was performed using Edwards-Sinsky stability factors $\boldsymbol{\mu}$ and $\boldsymbol{\mu}$ prime, which are given by the following equations:

$$\boldsymbol{\mu} = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|} > 1 \quad (1)$$

$$\boldsymbol{\mu}' = \frac{1 - |S_{22}|^2}{|S_{11} - \Delta S_{22}^*| + |S_{12}S_{21}|} > 1 \quad (2)$$

Where $\boldsymbol{\mu}$ measures the distance between the center of the Smith chart and the nearest unstable point in the Γ_L–plan, while $\boldsymbol{\mu'}$ measures the same distance, but in the Γ_S–plan. According to Edwards-Sinsky stability criterion, the unconditionally stability is achieved where μ and μ', both are greater than unity.

Using the proposed stability circuit depicted in figure 2, the obtained results are shown in figure 3. As we can remark, because of the proposed stability circuit, the selected active device is unconditionally stable over the frequency band ranging from 1 GHz to 6 GHz.

2.4 Load-pull simulations

In this work, the proposed matching networks are designed using the load-pull matching technique. The initial load-pull results are illustrated in figure 4.

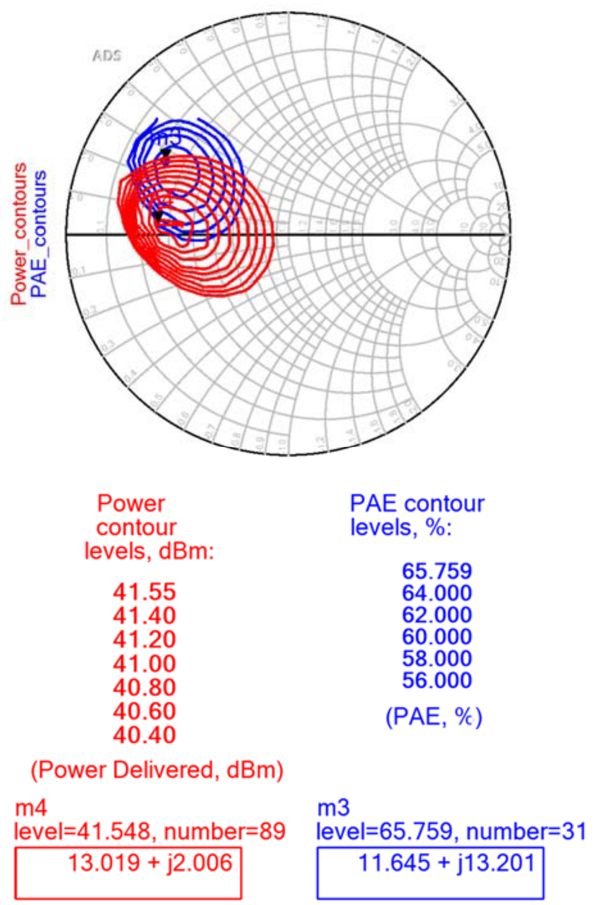

Fig. 4. Initial load-pull simulation results: PAE and delivered power contours with the output impedance for whether maximum PAE or maximum output power

Before starting the matching networks design, we need information about the active device input/output impedances that permit to achieve the design specification goals.

In fact, in order to achieve the high output power with the maximum possible efficiency, the output matching network for a power amplifier is designed to be low loss. However, to reaches this goal, the right active device output matching that can balance the high output power with the maximum possible PAE must be determined before. For that reason, the load-pull simulation is used in this work.

The initial load-pull simulation results are illustrated in figure 4, in which the delivered output power and the PAE contours, the appropriate output impedance that allows the high output power and the one that permits the maximum possible PAE are presented.

From that figure, and using the selected active device (Cree CGH 40010), the maximum PAE that can be reached is around 66%, and it can be achieved using the active device output impedance of 11.6 + j*13.2 Ω. On the other hand, the maximum output power that the active device can deliver is around 41.55 dBm, and it can be reached using an output impedance of 13 + j*2 Ω. The further information obtained from the initial load-pull simulation are presented in figure 5 and 6 respectively.

PAE_at_MaxPower	Gain_at_MaxPower	Pdel_dBm_Max
57.023	12.589	41.589

Zload_at_MaxPower	Z_In_at_MaxPower
13.189 + j1.883	5.696 + j4.211

Fig. 5. Input/output impedances for maximum output power (from the initial load-pull simulation results)

Pdel_dBm_at_MaxPAE	Gain_at_MaxPAE	PAEmax
39.965	10.965	65.825

Z_In_at_MaxPAE	Zload_at_MaxPAE
5.745 + j4.924	11.632 + j13.092

Fig. 6. Input/output impedances for maximum PAE (from the initial load-pull simulation results)

From figure 5, using 13.2 + j*19Ω as an input impedance and 5.7 + j*4.2Ω as an output impedance, we can reaches the maximum possible gain and output power, while using 5.7+j*5Ω (@ input) and 11.6+j*13 Ω (@output) instead, we can achieve the maximum possible PAE.

On the other hand, if information about the gain compression and the IP3 are required, the initial load-pull simulation is not enough. In this case, the 3-dB load-pull simulation is used.

In this work, after performing the 3-dB load-pull simulation, the adopted input/output impedances are the following:

- @ input side: $Z_S = 6.5 - j * 3.8\ \Omega$
- @ Output side: $Z_L = 28 + j * 0.5\ \Omega$

The adopted impedances allow achieving a maximum output power of 41.45 dBm with a PAE of 57% and large signal gain around 12.7 dB.

2.5 The proposed biasing and input/output matching networks

In this work, the proposed biasing and matching networks are designed using microstrip sections and implemented on Rogers RO4350B. The biasing circuits are designed to be an integral part of the matching networks. Referring to the biasing circuits, the RF choke is designed using λ/4 transmission line. The later dimensions are calculated around the frequency center of the operating frequency band. The proposed biasing and input/output matching circuits are illustrated in figure 7 and 8 respectively.

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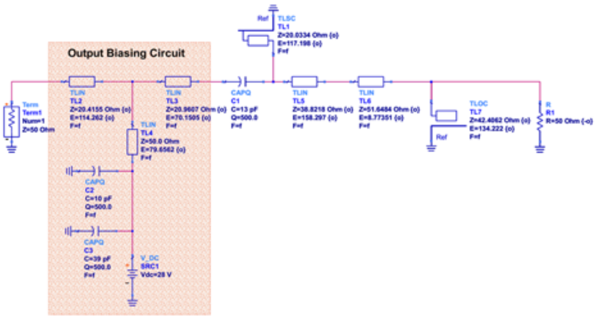

Fig. 7. The proposed output matching network.

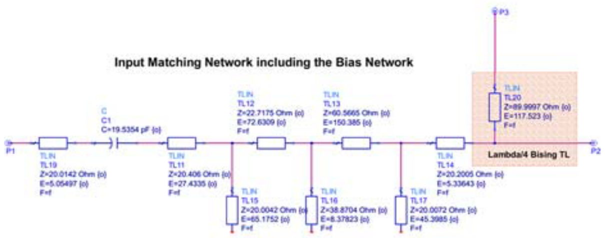

Fig. 8. The proposed input matching network

The output matching circuit depicted in figure 7 was designed using a special matching technique. In fact, the adopted active device output impedance obtained from the load-pull simulation is 28 + j*0.5 Ω. So, the output matching network aims is to match the output port 50Ω with the adopted active device output impedance. However, this latter is in Z format. Therefore, in order to use it as a target impedance, we need first to transform the S_{11} parameter of the proposed output matching network into Z format, then we perform an optimization process on the proposed output matching network with the aim to achieve the target output impedance obtained from the 3-dB load-pull simulation. On the other hand, the proposed input matching circuit illustrated in figure 8 is synthesised using the smith chart utility basing on the input matching impedance obtained from the 3-dB load-pull simulation.

2.6 The proposed PA circuit

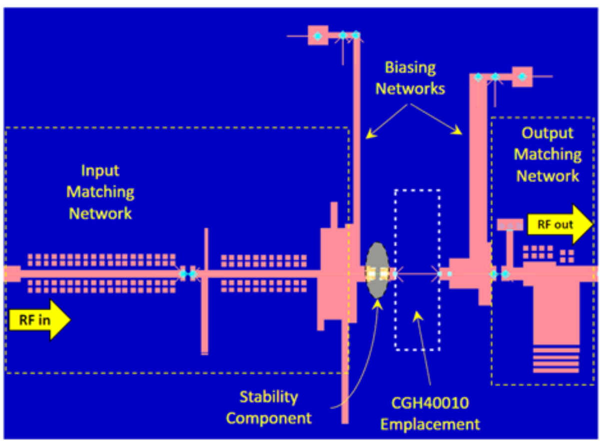

Fig. 9. The proposed PA circuit

The proposed PA circuit is shown in figure 9 in which all proposed networks in terms of biasing, input/output matching and stability networks are placed. The active device used in this work has a screw-down package, so it emplacement left free. The small square microstrip sections are added for after fabrication tuning purposes.

3 Results and discussion

In this section, the obtained results are presented and discussed. The characterization and validation of the proposed PA is partitioned into several steps. The first one consists of performing the small signal simulation. The latter allows checking small signal performances in terms of reflexion coefficients, the small signal gain, the reverse isolation coefficient and stability. The next step consists of performing the EM CoSimulation. This latter provides the closest result to the real performances. Thereafter, we will conclude with the nonlinear simulation. The aim of this simulation is to validate the nonlinear performances in terms of output power, the third order intercept point (IP3) and inherently the linearity, and the drain efficiency and power added efficiency (PAE).

3.1 Small-signal simulation results

As mentioned above, the Edwards-Sinsky stability factors (μ and μ prime) are used in this work for the stability analysis. The obtained results are depicted in figure 10. From that figure, we can remark that both μ and μ prime are greater than unity, therefore, the proposed PA is unconditionally stable over the entire operating frequency band ranging from 2.15 GHz to 2.65 GHz.

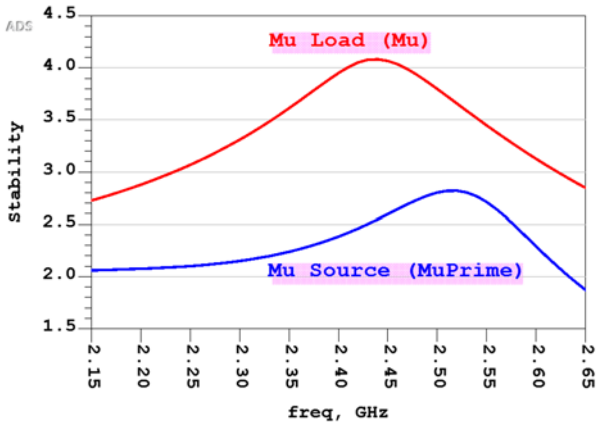

Fig. 10. Stability analysis of the entire PA circuitry over the frequency band ranging from 2.15 GHz to 2.65 GHz.

On the other hand, because of the neatly designed matching networks, the proposed PA achieves excellent matching performances. As illustrated in figure 11 and 12, from the schematic simulation, the proposed PA shows excellent input/output reflexion coefficients performances with an input return loss (under -16 dB) and an output return loss (under -18 dB) over the entire operating frequency band. However, comparing the schematic simulation results with the co-simulation, the latter shows a slight degradation of the input/output return loss performances, but we still achieving excellent matching performances.

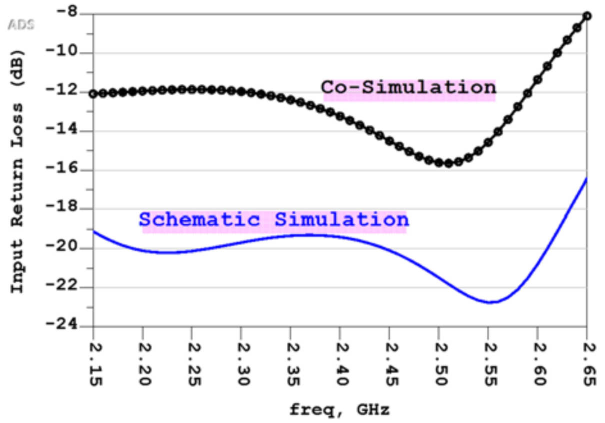

Fig. 11. Input return loss versus frequency.

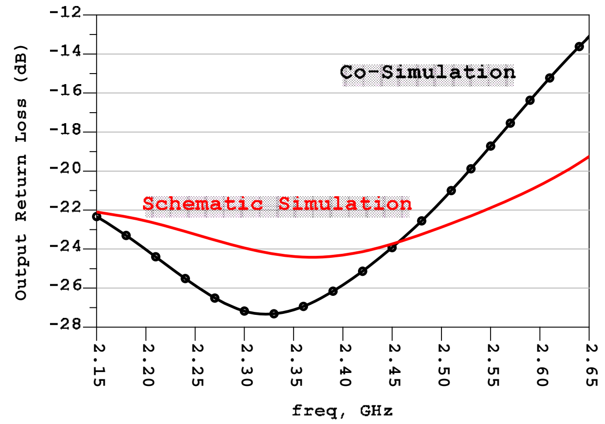

Fig. 12. Output return loss versus frequency.

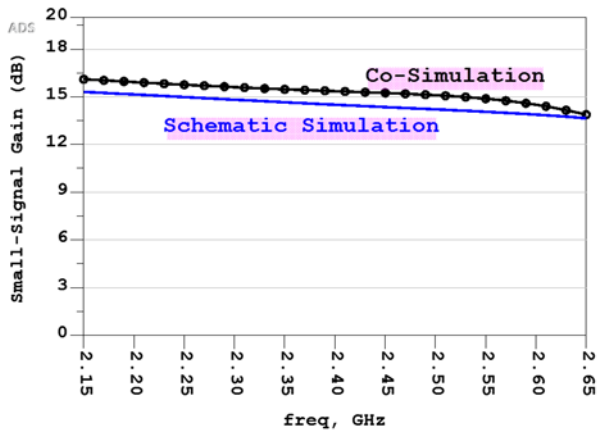

Fig. 13. Small-signal gain versus frequency.

From figure 13, the proposed PA reaches an excellent flat small signal gain around 15 dB over the entire operating frequency band from 2.15 GHz to 2.65 GHz. In addition, the schematic simulation result is very close to co-simulation performance.

3.2 Nonlinear performances

In this subsection, the nonlinear performances in terms of gain compression (figure 14), output power (figure 15), PAE (figure 16), drain efficiency (figure 16) and the IP3 (figure 17) are presented and discussed.

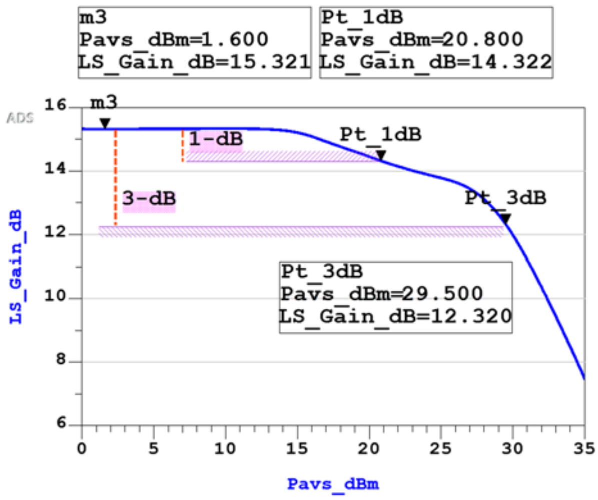

Fig. 14. Large signal gain versus input power

From figure 14, the proposed PA reaches an excellent large signal gain around 15 dB. In addition, the required input power to achieve the 1-dB compression point is about 20.8 dBm, while we need a 29.5 dBm as input power to reach the 3-dB compression point.

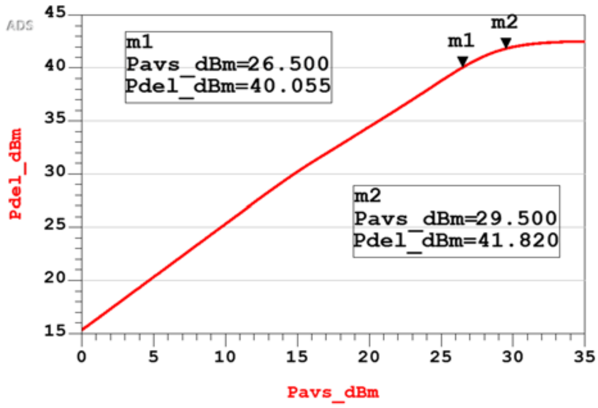

Fig. 15. Output power versus input power

On the other hand, the proposed PA achieves a saturated output power around 42 dBm (15 watts) as depicted in figure 15. In addition, at 1-dB compression point, the output power achieved is around 40 dBm, while the output power at 3-dB compression point is near than 42 dBm.

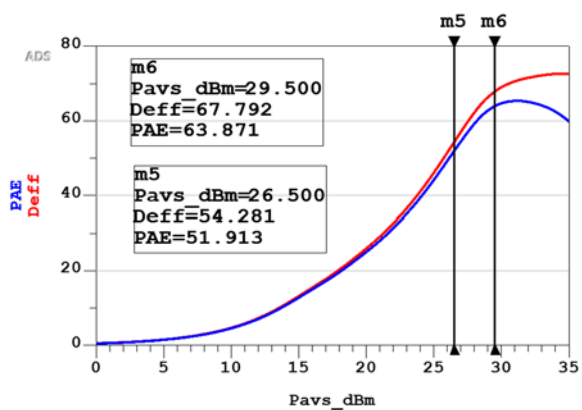

Fig. 16. PAE and drain efficiency versus input power

In terms of efficiency, the proposed PA touches a maximum PAE around 65% with a maximum possible drain efficiency of 75% as illustrated in figure 16.

Besides, at 1-dB compression point, the proposed PA achieves a PAE of 51% with a drain efficiency of 54%. However, at 3-dB compression point, the PA provides a PAE around 64% with a drain efficiency of 67%.

In terms of linearity, the third order intermodulation products as well as the intercept IP3 results are illustrated in figure 17. Referring to the third-order intermodulation products, the intercept IP3 is defined as the point where the power in the fundamental tone and the third order product are equal if the amplifier is assumed to be linear.

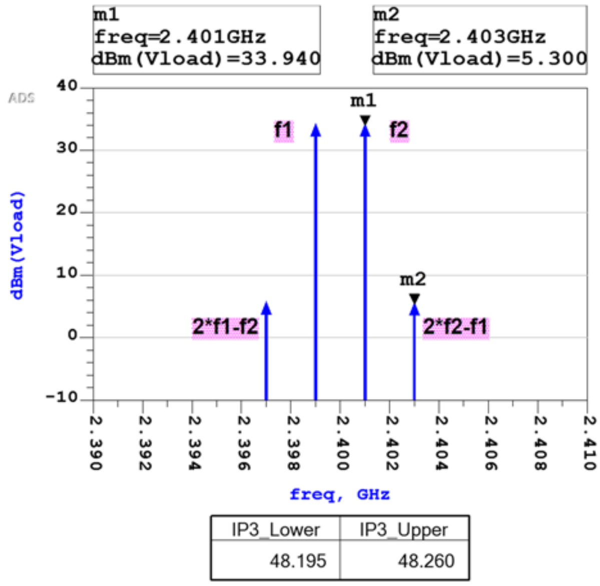

Fig. 17. Two-tone simulation analysis {f_1: 2.399 GHz, f_2: 2.401 GHz}.

From the two-tone simulation results illustrated in figure 17, the proposed PA shows an excellent output intercept IP3 around 48 dBm, which is an excellent linearity performance.

3.3 Benchmarking

Table 1 compares the proposed PA performances with the contemporary published works.

From table 1, the proposed PA is well positioned compared to recently published works. In fact, the proposed output impedance matching network as well as the selected bias point allow reaching excellent nonlinear performance in terms of output power output, PAE and OIP3. Compared to the contemporary published works, the proposed PA provides a wide bandwidth around the 2.4 GHz ISM band with an excellent output power and OIP3 using only one stage.

Table 1. Performances comparison of the proposed PA with contemporary published works

	[15]	[17]	[18]	[20]	This work
Freq. [GHz]	2.19	2.4	2.14	2.6	2.15 – 2.65
# Stage	2	2	2	2	1
Gain [dB]	23	15	16.6	7.5	15.35
Pout @ 3-dB [dBm]	38	37.3	36.9	41.63	41.34
PAE @ 3-dB [%]	70	63.3	55.7	49.48	64.64
DE [%]	75	68	57.0	58.2	71.94
OIP3 [dBm]	NA	NA	NA	NA	48

4 Conclusion

In this paper, a high output power and high efficiency power amplifier (PA) operating in the frequency band ranging from 2.15 GHz to 2.65 GHz is presented. The proposed PA is based on Cree CGH40010 GaN active device and implemented on Rogers RO4350B substrate.

The proposed input/output matching networks are designed based on the load-pull matching technique. The biasing circuits are designed to be an integral part of the matching networks. The RF choke used in the biasing circuitry was designed using λ/4 microstrip section. The latter dimensions were calculated around the 2.4 GHz ISM band.

In terms of performances, the proposed PA achieves an unconditionally stability over the entire operating frequency band ranging from 2.15 GHz to 2.65 GHz with excellent impedance matching performances. If fact, with the neatly designed input/output matching networks, the proposed PA reaches excellent input/output reflexion coefficients, both are under -16 dB over the entire operating bandwidth, with an excellent gain of 15 dB.

In terms of nonlinear results, the proposed PA provides a saturated output power around 42 dBm, which leading to about 15 watts, with a PAE around 63% and a drain efficiency nearby to 68% at 3-dB compression point. In terms of linearity, the proposed PA shows an excellent output intercept IP3 of 48 dBm.

A PA with the introduced performances would be very suitable for many applications operating around the 2.4 GHz ISM band that are require a high output power along a high efficiency such as radars, WCDMA, the modern and next generation wireless communication systems.

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