Homogeneous, lossy and Asymmetrical Strip Line with tabbed design for High-Speed Interface application

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Abstract. Reduction of cross talk noise is an important characteristics of clean signal quality for high-speed channel analysis. In this paper, tab added strip line is modelled to improve signal distortion in high-speed digital circuits. A comprehensive analysis of the proposed design is done across frequency domain and time domain. 6dB improvement of FEXT is observed during frequency domain analysis and 3mV in eye height of time domain analysis.

1 INTRODUCTION

With the increasing demand for higher data rates and bandwidth in modern digital systems, the need for high-speed digital circuits that can handle the increased data transfer rates has become a critical issue. However, as data rates increase, signal integrity becomes a significant challenge that needs to be addressed to ensure the reliable operation of high-speed digital circuits. Signal integrity issues such as signal distortion, noise, and crosstalk can severely impact the performance of digital circuits, leading to errors and data loss. Stripline provides better isolation between adjacent traces due to the grounded planes on either side of the signal trace. This can be important in high-density circuits to prevent crosstalk and signal interference. Stripline has lower signal loss than microstripline because the signal is confined between two grounded planes, which reduces radiation loss and increases signal integrity.

To address these challenges, various techniques have been proposed to improve the signal integrity of high-speed digital circuits. In [1] a novel layout design for single-ended stripline minimizes the crosstalk. In [2] guard trace stubs between the parallel lines of the serpentine delay line have been used to mitigate the same. Tab routing is also one of the methodologies used to enhance signal integrity and minimize signal distortion. [3] [4] [5].

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In this paper, we propose the use of stripline with tabbed lines as a means of improving the performance of high-speed digital systems. We conducted a comprehensive analysis of the proposed design, including the frequency domain and time domain. Stripline with tabbed lines is a technique that utilizes metal tabs along the signal path to reduce signal distortion and improve signal integrity in high-speed digital circuits.

In Section II of this paper, the different models used in the study are introduced. The models include the conventional design and the proposed tab-routed design. Section III presents a detailed analysis of the performance of these designs in both frequency domain and time domain. The frequency domain analysis involved comparing the S-parameter behavior of the designs up to 20 GHz. In the time domain analysis, eye height (EH), and eye width (EW) were compared for different models. The eye diagram is a powerful tool for visualizing the quality of the transmitted signal and is used extensively in high-speed digital circuit design to ensure signal integrity. The comparison of these parameters provides valuable insights into the performance of the designs It highlights the effectiveness of the proposed tab-routed design in reducing signal distortion and improving signal integrity in high-speed digital circuits.

2 MODELLING

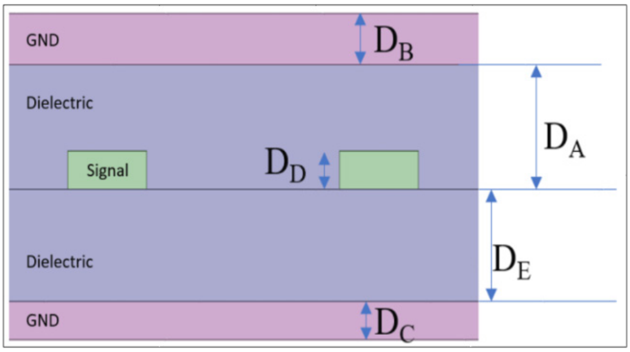

Fig. 1. Side view of conventional stripline design.

The structures with three kinds of stripline are shown in Fig. 2. Conventional stripline and one-sided tab stripline and both-sided tab stripline are presented in Fig. 2(a), 2(b), and 2(c), respectively, with the geometrical parameters of line width w for conventional is 0.098mm and 0.075mm for other two tabbed cases. Tab width b is 0.02 mm for Fig. 2(a) and b/2 is 0.01mm for Fig. 2(c). Trace thickness t which is also D_D from fig. 1 is 1.2mil, tab length a is 2.460mil for fig. 2(a) and 3.93mil for fig. 2(b), and e-to-e (edge to edge) space is 0.436mm for all cases, dielectric constant (D_r) is 3.8, loss tangent of 0.014. By setting w mm, the characteristic impedance was close to 36ohm for tabbed and 40ohm for conventional.

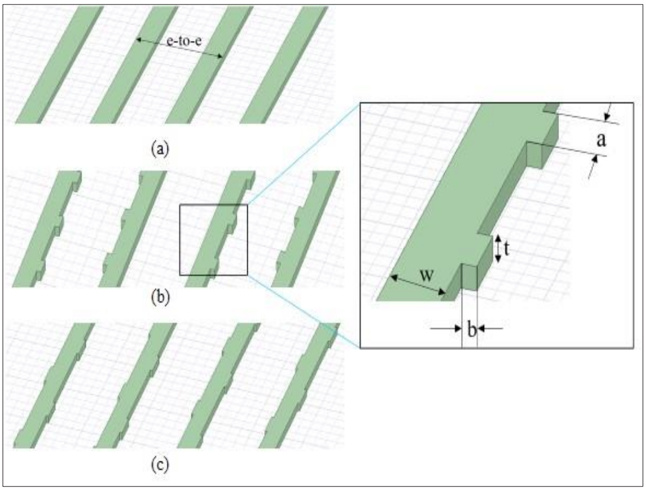

Fig. 2. 3D views: (a) conventional stripline design, (b) one-sided tab stripline design. (c) both sided tab stripline design.

Within this section, a comparison was made between the conventional stripline design and the tab routing design.. In this work, the side view of traditional striplines with copper traces as shown in Fig.1 is routed between dielectric. The dielectric has a relative permittivity of 3.8 and a loss tangent of 0.014. Fig.2(b) and 2(c) illustrate the two various models that are used in this research.

Table 1. Tab routing specification

D_A	3.9mil	e-to-e	17.16mil
D_B	1.6mil	D_E	3.5mil
D_C	1.2mil	D_D	1.2mil

3 ANALYSIS

Within this section, two essential analyses were conducted, namely frequency domain analysis and time domain analysis.

3.1 Frequency domain analysis

For frequency domain analysis the simulation is carried out using the tool ANSYS HFSS [6] and the sweep frequency used till 20 GHz. At first the conventional model is simulated and corresponding TDR (time domain reflectometer) impedance, FEXT, IL is noted. Then the tabs were optimized for other two cases in such a way to get TDR impedance close to conventional design and at the same time maximum improvement in FEXT, IL. For comparison of these s-parameters curves for all the cases are plotted. The worst cases have been considered for comparison of all the models.

Fig.5 illustrates the graphs containing curves for all the three cases. The curve for conventional design shows higher fluctuations than the curves having tabbed design which are smoother than the former. The second comparison is for the FEXT, and the Fig.6 shows the graph comparison of all the cases. Here also it can be seen that the curve for tabbed design stays lower than the conventional design.

3.1.1 FEXT improvement – Mathematical expression

The configuration of a stripline in a single-ended setup is mainly affected by edge-coupled FEXT, which is the most significant source of noise that affects the overall performance of the system. The following equations are typically used to provide the best characterization of FEXT in general[1]:

$$Fext = \frac{1}{2}(KC - KL)\frac{l}{v_p}\frac{v}{t_r} \quad (1)$$

$$KC = \frac{C_m}{C_m + C_S} \quad (2)$$

$$KL = \frac{L_m}{L_m + L_S} \quad (3)$$

$$TD = \frac{l}{v_p} \quad (4)$$

$$Fext = \frac{TD}{2}\frac{v}{t_r}\left(\frac{C_m}{C_m + C_S} - \frac{L_m}{L_m + L_S}\right) \quad (5)$$

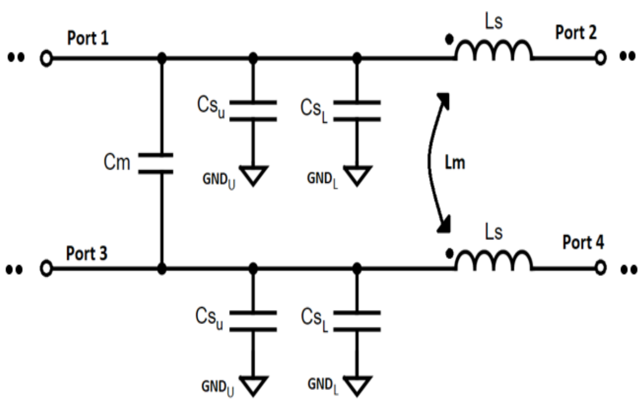

Fig. 3. Equivalent circuit model for conventional stripline

FEXT is generated in single-ended striplines due to the interaction between the conductors, which occurs via both mutual capacitance and mutual inductance, resulting in coupling through electric and magnetic fields. The extent of FEXT can be measured by taking into account several parameters, including the length of the conductors (l), applied voltage (v), propagation velocity (vp), rise time of the signal (tr), coefficient of capacitance (KC), and coefficient of inductance (KL). KC represents the proportion of mutual capacitance (Cm) to total capacitance, where total capacitance is the sum of mutual capacitance and self-capacitance of the stripline (Cs), as illustrated in equation (2). Similarly, KL can be defined as the ratio of mutual inductance (Lm) to total inductance, where total inductance is the sum of mutual inductance and self-inductance of the stripline (Ls), as shown in equation (3). The time delay TD (which is the ratio of overall length and propagation velocity) in equation (4), the FEXT of single-ended striplines can be expressed using equation (5).

Equation (5) implies that to eliminate FEXT, the ratio of the coefficient of capacitance to the coefficient of inductance should be equal, resulting in a zero difference. This is because achieving a true zero-time delay and applied voltage in a real system is impossible. If the stripline configuration is ideal, with uniform dielectric materials surrounding the stripline, then the coefficient of capacitance and coefficient of inductance would be the same, resulting in zero FEXT. However, in real PCB designs where the dielectric environment is not perfectly homogeneous, the capacitance ratio and inductance ratio are not equal in magnitude. As a result, FEXT still exists in single-ended stripline configurations.

Unlike microstripline, stripline has two ground plane therefore it will have two self-capacitance CsU and CsL with respect to upper ground and lower ground plane respectively. In a typical stripline design, adding tabs increases the value of Cm. However, in tabbed stripline designs, reducing the trace width to match the TDR impedance helps decrease Cs, which then increases Cm/ Cm+Cs ratio as per equation (5). And this term $\frac{C_m}{C_m+C_S} - \frac{L_m}{L_m+L_S}$ will be close to zero.

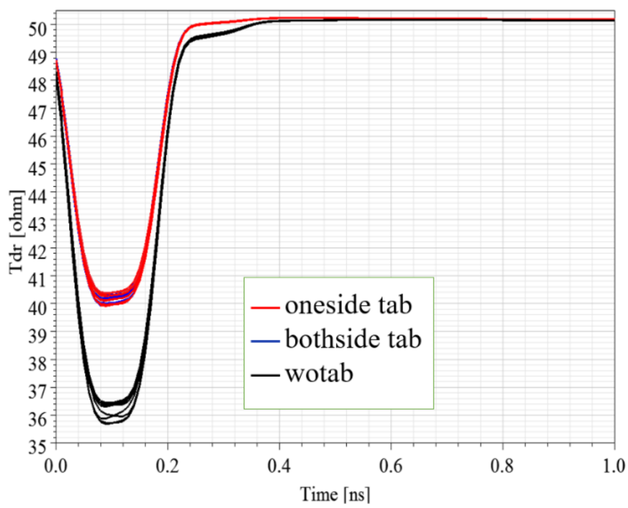

Fig. 4. Comparison of TDR impedance for conventional and tab routed.

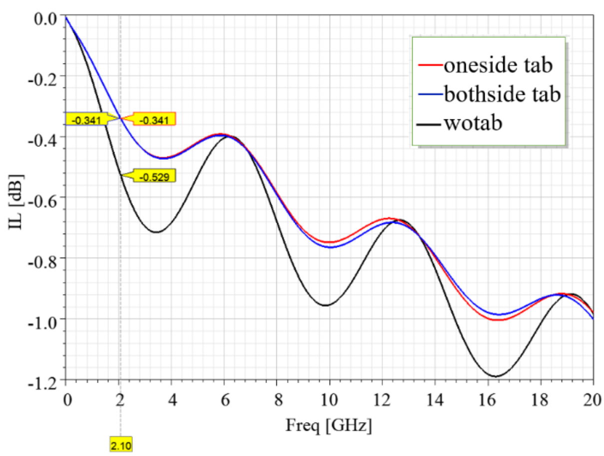

Fig. 5. Comparison of insertion loss (IL) for conventional and with tab routing stripline.

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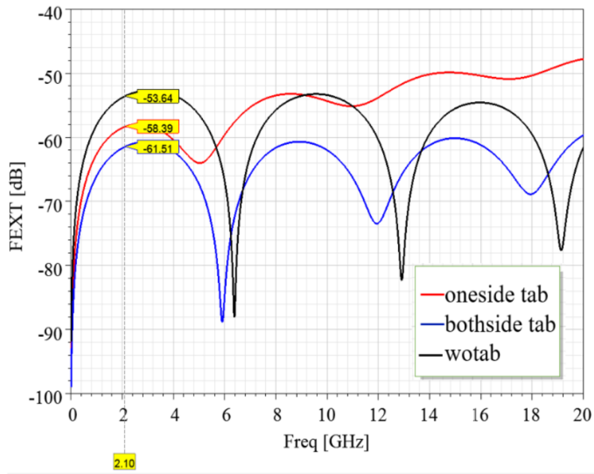


Fig. 6. Comparison of far end crosstalk (FEXT) for conventional and with tab routing stripline.

3.2 Time domain analysis

In the time domain analysis, S-parameter files is used to generate the eye diagrams using ADS. The eye diagram is a graphical representation of a digital signal's quality and is commonly used to evaluate the performance of high-speed digital circuits. The eye diagram shows the amplitude and timing jitter of the signal at the receiver, which allows for the characterization of the system's noise and distortion.

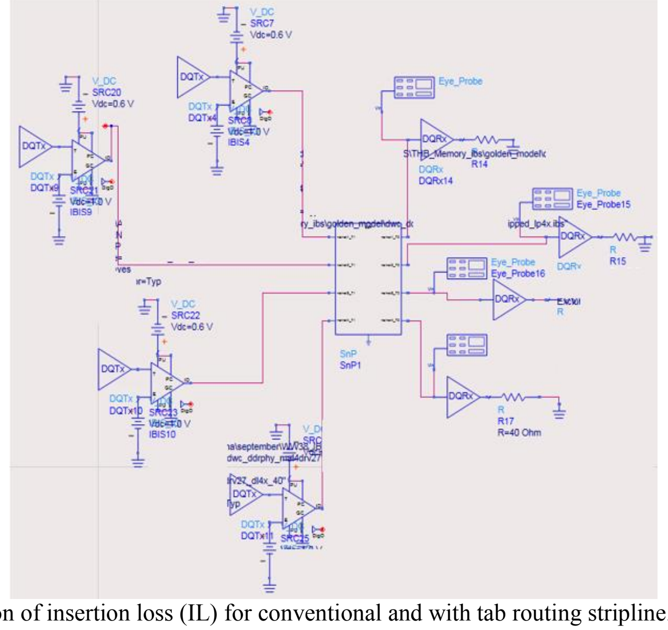
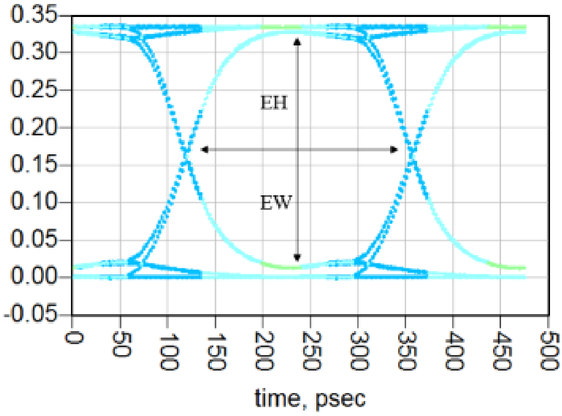
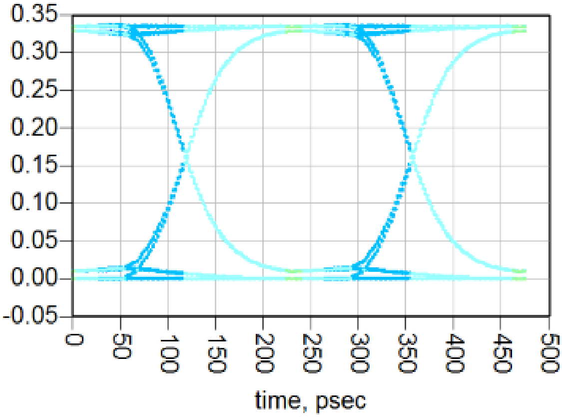


Fig. 7. Comparison of insertion loss (IL) for conventional and with tab routing stripline.

Fig.7. shows the circuit model use to produce the eye diagram. It consists of IBIS models connected to every port of s-parameter at transmitter side and receiver side. Here, a data transfer rate of 4200 megabits per second and a rise time of 100 picoseconds are being utilized.



(a)conventional



(b)bothside tab

Fig. 8. Comparison of insertion loss (IL) for conventional and with tab routing stripline.

Table 2. Specification for Eye diagram

Speed (4200Mbps)	EW (ps)	EH (mV)
Conventional	234.5	312
Oneside tab	234.5	315
Bothside tab	236.9	316

Fig. 8. shows eye diagram comparison for conventional and both-side stripline. The generated eye diagrams showed significant improvements in signal quality, with a reduction in jitter and an increase in signal amplitude. Table II shows the 1.28% improvement in eye height and 1.02% in eye width when compared with conventional to both side tab design. These

improvements are indicative of the reduced signal distortion and improved signal integrity that was observed in the frequency domain analysis.

Overall, the results of the time domain analysis confirm the effectiveness of the proposed design in improving the performance of high-speed digital systems. The use of S-parameter files and in the analysis allowed for a more accurate simulation of the system's behavior and provided valuable insights into the performance of the design.

4 CONCLUSION

This paper has demonstrated the effectiveness of using stripline with tabbed lines. 8dB improvement in FEXT and 4mV improvement in EH has been observed. The simulation modelling results showed significant improvements in frequency domain parameters such as IL and FEXT. The time domain analysis also showed improvements in signal quality, with the tab routed design exhibiting a larger eye height and wider eye width compared to the conventional design.

References

1. H. Lin, B.-C. Tseng, and J. Yen, “NDWMFCOSES,” in *2017 IEEE International Symposium on Electromagnetic Compatibility & Signal/Power Integrity (EMCSI)*. IEEE, (2017), pp. 261–266.
2. G.-H. Shiue, J.-H. Shiu, P.-W. Chiu, Z.-H. Zhang, M.-N. Yeh, and W.C. Ku, “IOTDTWAEDOSDLUGTSISS,” in *19th Topical Meeting on Electrical Performance of Electronic Packaging and Systems*. IEEE, (2010), pp. 249–252.
3. R. K. Kunze, Y. Chu, Z. Yu, S. K. Chhay, M. Lai, and Y. Zhu, “CMIMUTL,” *Intel white paper*, (2015).
4. K. Song, S. Lee, and S. Ahn, “TRMDOFHSSC,” in *2022 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*. IEEE, (2022), pp. 34–34.
5. W. Jiang, X.-D. Cai, B. Sen, and G. Wang, “EBSTCALANMLFTA,” *IEEE Transactions on Electromagnetic Compatibility*, **61**, no. 2, pp. 548–557, (2018).
6. ANSYS tools and support 2022R2 version: www.ANSYS.com.
7. ADS tools and support 2021version: https://www.keysight.com.