The Design of An LDO Regulator

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Abstract- **In today's modern systems on chip (SOCs), a crucial power management circuit is the low-dropout (LDO) regulator. Of course, the need for supply voltage regulation, goes back many years in the past since the circuits have been designed. Today, LDO based voltage regulators are frequently used in a number of mixed-signal systems to produce local supply voltages that feed different building blocks. LDOs try to isolate the noise of the circuit and noise from the global supply and try to reduce their effect on device performance. For the state of desired achievement, each LDO's architecture is circuited to the specific cell it feeds. An LDO designed to feed a flash analog-to-digital converter, for instance, differs greatly from one designed to input a VCO. In this paper, we direct an LDO for a VCO of 5-GHz *LC* and point the particulars of 1.2 V as input voltage, produces 1V as output voltage, 5 mA of maximum output current, power supply rejection greater than 40 dB up to 10 MHz and noise voltage present at output that is less than 25nV/ $\sqrt{\text{Hz}}$ at 1 MHz.**

***Keywords*--** **systems-on-chip, SOC, regulator, LDO, noise, mixed-signals, Power supply rejection.**

Introduction:

The Need for LDOs: - A system-on-chip associate a number of building blocks. Some of them are sensitive to supply voltage changes and excursion and some of them are that of noise from the supply and some introducing grievous noise on their supply wires caused by intrinsic ripples. As a result, voltage regulators are required, which produce a stable voltage even when the input voltage varies. The remaining components of the SOC are supplied with this, set output voltage as source. Voltage regulators come in two primary varieties: linear and switching. LDOs are linear regulators that are commonly used in SOCs. The reduction in supply voltage due to scaling has made LDOs an important component of power management SOCs because we require lower input-output voltage differences, that is, low dropout (LDO). Let's consider the following *figure (1)* how an LDO is providing a constant supply out of the global supply to the nonexclusive successive-approximation-register (SAR) analog-to-digital converter (ADC). A feedback loop is formed by the comparator, and the logic component, the digital-to-analog converter, that successively tries to update V_{DAC} so that it approaches V_{in}. In this paper, we design an LDO which consists of mainly four parts: an error amplifier (op amp), a pass element, a feedback network, and a load. Consider the basic comprehensive negative feedback system voltage regulator structure in the *figure (2)*. The unregulated, input possibly containing noise, V_{in}, operational amplifier (op-amp) controls the current flow of a pass transistor when voltage, V_{in}, is applied to it such that

$$V_S = V_{out}R_2/(R_2 + R_1) \tag{1}$$

persists close to V_{REF} . In modern day's LDO design, one would prefer to conduct the dropout, $V_{in} - V_{out}$, no more than or equal to 200 mV. In addition to the dropout, a collection of other specifications become demanding in on-chip LDOs. **1)** PSRR, power-supply rejection ratio, which is also known as line regulation, formulated as, $dV_{out}/\ dV_{in}$, effect emerges from two routes, the pass transistor and the source of A_1. **2)** Output noise, $V_{n,out}$: The LDO itself produces noise at the output in the absence of input noise, which is a severe issue, if, for instance, the reference generator in *figure (1)* is perceptive to noise in its supply voltage, and so appears in the result and may degrade. **3)** Load regulation, formulated as $dV_{out}/\ dI_L$ in *figure (2)*: The transient currents can cause a noticeable jump in the other blocks of LDO output voltages even when the bias currents in the reference generator in figure (1) are comparatively quiescent. The output impedance of the LDO is directly proportional to this effect. Following that, we propose that load regulation weakens at high frequencies. **4)** Area and power dissipation: When a SOC uses a high number of LDOs for varied purposes, both of these factors are of utmost importance.

We should also point out that some of the aforementioned specifications may exhibit a poor phase margin (PM) linked to the LDO's feedback loop. For instance, in specific frequency bands, it may worsen load regulation, introduce peaks in $V_{n,out}$, and degrade PSRR.

Selection of Pass Transistor:

The pass transistor in *figure (2)* can do the work of a current source. It can also act as a source follower. Each of these choices has their own advantages and disadvantages in terms of the dropout voltage, PSRR, load regulation, and output noise. So, selection of pass transistor is also crucial.

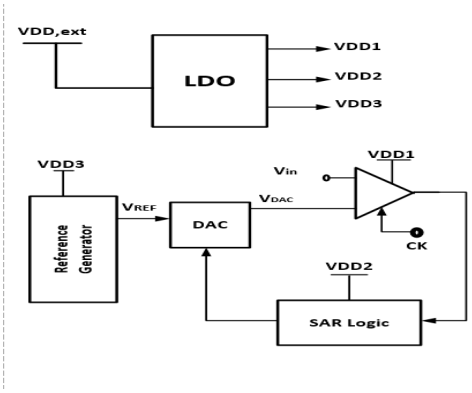

Figure (1): SAR ADC.

Either an NMOS or a PMOS device may serve as the pass element. PMOS devices are driven from a signal that is negative with respect to the input, whereas NMOS devices need a positive drive signal with respect to the output. At low input voltages, producing a positive driving signal becomes challenging. As a result, P-type devices are frequently used to create LDOs that run from low input voltages. Throughout our analysis we will consider P-type or controlled current source type as pass transistor [5]. However, N-type or voltage follower, provides better PSRR. Also, if we neglect the channel-length modulation in M_1, it leads to $d\ V_{out}/\ d\ V_{in} \rightarrow 0$. This is due to the fact that while a transistor is functioning in the saturation region, changes in the drain voltage do not depend on the source voltage. Let's initiate our analysis with the circumstances in *figure (3.a)* where the PMOS device, M_1, is operating in saturation region. It serves as a controlled current source in this instance. The source-drain voltage of M_1 is equal to the dropout, $V_{in} - V_{out}$. By selecting a broad transistor, this dropout can be reduced to a minimum. We want to figure out $d\,V_{out}/\ d\,V_{in}$ and $dV_{out}/\ dI_L$.

Here, we rely on the infinite supply rejection of op amp A_1 for simplicity. We must first get the loop gain, A_{LG}, in order to address this side. Breaking the loop at S provides a small-signal resistance, R_L, if we relate it to the load, formulates

$$A_{LG} = A_1 g_{m1}[R_L \| (R_1 + R_2)]\frac{R_2}{R_1+R_2} \tag{2}$$

The transconductance of M_1 is correspondingly advanced by the op-amp. To find $d\,V_{out}/\ d\,V_{in}$, we set up the small -signal model shown in figure (3.b). Now, M_1 feels a gate-source voltage equal to $[A_1R_2/(R_1 + R_2)]V_{out} - V_{in}$ and, thus, generates a small-signal current formulated as below

$$I_{D1} = g_{m1}\left(\frac{A_1R_2}{R_1+R_2}V_{out} - V_{in}\right). \tag{3}$$

Beginning with passing through $R_L||(R_1 + R_2)$, this current converts $-V_{out}$. It accompanies that

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}[R_L||(R_1+R_2)]}{1 + A_1 g_{m1}[R_L||(R_1+R_2)]\frac{R_2}{R_1+R_2}} \tag{4}$$

$$= \frac{g_{m1}[R_L||(R_1+R_2)]}{1 + A_{LG}}. \tag{5}$$

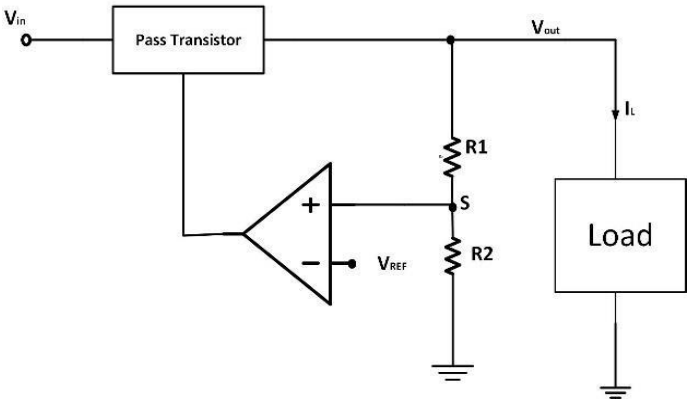

Figure (2): A basic LDO topology.

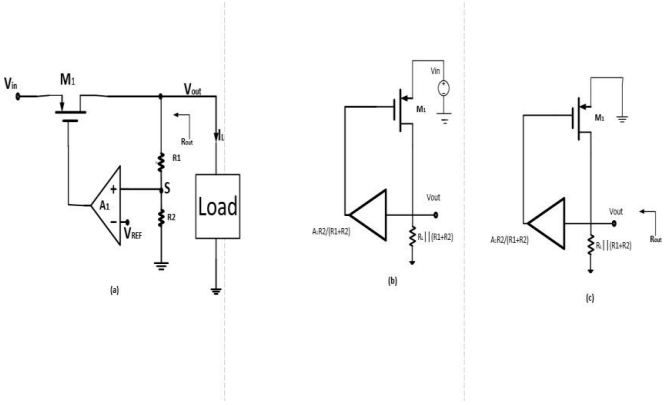

Figure (3): (a) Controlled-current source used in LDO. (b) PSRR formulating model, and (c) and corresponding model for calculation of Thevenin's output impedance.

Without any doubt, by watching M_1 and $R_L||(R_1+R_2)$, that is subsequently put into a negative feedback loop, we may also foresee this outcome. It then encounters that the gain is minimised by a factor of 1+ A_{LG}. Generally, $A_{LG} \gg 1$, so

$$\frac{V_{out}}{V_{in}} \approx (1+\frac{R_1}{R_2})\frac{1}{A_1} \tag{6}$$

indicating that the PSRR can be enhanced by increasing A_1. Now, to address load regulation, $dV_{out}/\ dI_L$, we can say, that this quantity, in fact, is nothing but the Thevenin's impedance of the LDO, R_{out}, seen from the output in *figure (3.a)*. Constructing the circuit as in *figure (3.c)*, we examine that M_1 assume like a diode-connected device but with a transconductance enhanced to $g_{m1}A_1R_2/(R_1+R_2)$, we have

$$R_{out} = \frac{1}{g_{m1}A_1\frac{R_2}{R_1+R_2}}||(R_1+R_2). \tag{7}$$

The first term in the parallel combination is much less than the second, yielding

$$R_{out} \approx (1 + \frac{R_1}{R_2}) \frac{1}{g_{m1}A_1}. \quad (8)$$

From the perspective of load regulation, we must amplify A_1 too. This is because as A_1 increases, it reduces R_{out} in (8), and, in turn, with this, the LDO has better load regulation and thus it can act as a, probably, better voltage source for the next stage it drives. We must choose the pass transistor's *(W/L)* parameters such that they must be at least (*100µ/30 nm*), as the pass transistor in this design must generate a load current of no more than 5 mA that flows through the feedback network, for a drain current of 6 mA and $|V_{DS0}|$ = 0.2 V. Also, all other transistors employed use the (*W/L)* equal to *(250µm/120nm)*.

Since, a practical pass-transistor of PMOS type in *figure (3.a)* marks a finite output resistance, r_{o1}, acknowledging V_{in} to percolate to V_{out} and degrades the PSRR. This phenomenon can be simply thought of as simple voltage division between r_{o1} and R_{out} (*figure (4)*) and can be formulated as

$$\frac{V_{out}}{V_{in}} = \frac{R_{out}}{R_{out} + r_{o1}} \quad (9)$$

$$= \frac{(1+R_1/R_2)}{g_{m1}r_{o1}A_1 + 1 + R_1/R_2} \quad (10)$$

where we have assumed $R_L \gg R_{out}$. This result is considerably lower than that in (6) by roughly a factor of $g_{m1}r_{o1}$ and, thus, can be ignored. Additionally interesting is the LDO output noise. We observe that V_{nM}^2 can be divided by A^2 and placed in series with V_{nA}^2 [*figure (5.b)*] when modelling the noise of M_1 by a gate-referred voltage, V_{nM}^2 and that of A_1 by an input-referred source, V_{nA}^2 [*figure (5.a)*]. The circuit produces $V_{n,out}^2$ by maintaining V_S near to V_Y with a high loop gain, given as in (11). By raising A_1, the contribution of M_1 is reduced. This equation can also readily include the noise caused by R_1 and R_2. Their noise can be modelled as $4kT(R_1||R_2)$, and noise from the band gap circuit present in V_{REF} in *figure (3.a)*. Two additional noise components, both are

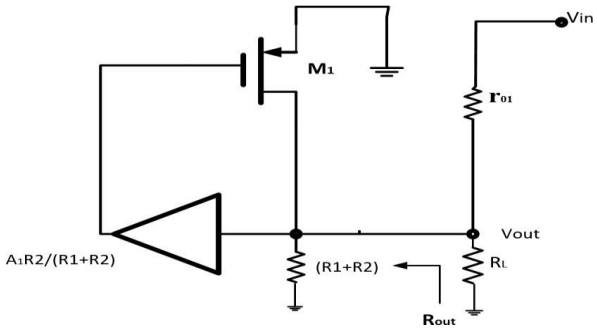

Figure (4): PSRR affected by transistor output resistance**.**

$$V_{n,out}^2 = (1 + \frac{R_1}{R_2})^2 (V_{nA}^2 + \frac{V_{nM}^2}{A_1^2}) \quad (11)$$

simply added to V_{nA}^2. If V_{in} or I_L in *figure (3.a)* contains high-frequency variation, then we must rethink of the results obtained previously and address them. Specifically, there is at least one pole in amplifier A_1. Therefore, we may swap out the gain A_1 in the previous equations for A_1 with $A_0/(1 + s/\omega_0)$, where ω_0 stands for the pole frequency. Thus, (6) changes to

$$\frac{V_{out}}{V_{in}} \approx (1 + \frac{R_1}{R_2}) \frac{1}{A_0} (1 + \frac{s}{\omega_0}), \quad (12)$$

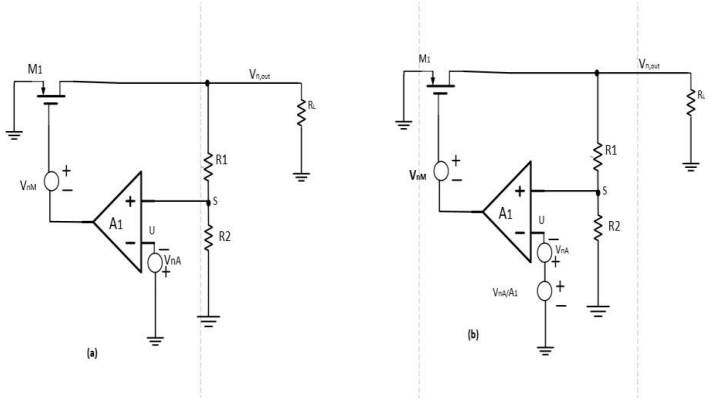

Figure (5): *(*a) Noise sources present in the LDO circuit and (b) noise of M_1 referred to the op amp input in the LDO.

and (8) changes to

$$Z_{out} \approx (1 + \frac{R_1}{R_2}) \frac{1}{g_{m1}A_0} (1 + \frac{s}{\omega_0}), \tag{13}$$

We will see in the upcoming figures that, the PSRR starts deteriorating and so does the load regulation beyond ω_0. Additionally, we anticipate significant time domain ringing at the output since the LDO displays an inductive output impedance. This is because the load contains capacitive components. And they help in drawing transient currents as they collectively resemble with the general second order system. Moreover, (11) exposes that the noise introduced by M_1 goes on enhancing as $|A_1|$ decays with frequency. If we run through, the extrinsically low-frequency LDO needs for a high-gain, broadband, low-noise op amps. For instance, with $\omega_0 = 2\pi(10MHz)$ and A_0 =100, the gain-bandwidth product of the op amp must be 1 GHz.

Op-Amp Requirements: -

Op-amp is the most important component of the LDO. It's choice and design are crucial for LDO and also in tackling with the stability problems. The op amp's performance has a significant impact on how well the LDO performs. The low-frequency PSRR is given by

$$\frac{V_{out}}{V_{DD}} = (1 + \frac{R_1}{R_2}) \frac{1}{A_1} \tag{14}$$

where it is expected that the loop gain is significantly bigger than unity [1]. If, for instance, V_{REF} = 0.9 V we get $1 + R_1/R_2 = 1/0.9$ and hence $A_1 > 100/0.9 \approx 110 \equiv 41$dB for PSRR $= -40$ dB. We assume that the op amp's open-loop 3-dB BW must be more than this amount of 10 MHz because the LDO is required to give a rejection ratio of 40 dB up to 10 MHz. Therefore, the unity-gain BW for a one-pole design is 110 x 10 MHz, or 1.1 GHz. It is intriguing that a decently broad op amp is required by an extrinsically low-frequency LDO. Because of this, we opt to employ only low-voltage transistors in the signal route of the op amp.

There may be a need for frequency compensation because, the op amp and pass transistor forming feedback loop have several poles because of intrinsic capacitors. That is why output node in *figure- (6)* has to undergo a number of trade-offs in this concern. First, if capacitor to node X is inserted in order to enhance the rejection ratio at high frequencies, the stability of the loop is compromised, demonstrating peaking in the PSRR. Second, if $R_1 + R_2$ is reduced, it draws more current and so does the power and boosting the corresponding pole frequency, dissipation of power rises. For the scenario of VCO of our concern here, C_{VCO} and $(R_1 + R_2)||r_{o1}$ seem to set a maximum limit for the pole frequency of node X. As an example, $C_{VCO} = 0.5$ pF and $(R_1 + R_2)||r_{o1} = 1$ kΩ collectively yield $\omega_X = 2\pi(318)\ MHz$. After applying frequency correction, the unity-gain bandwidth cannot be more than

this amount if the initial nondominant pole of the loop is ω_X. The previously decided 1.1-GHz target then seems to be out of reach. Pole-zero cancellation and pole splitting, fortunately, address this problem.

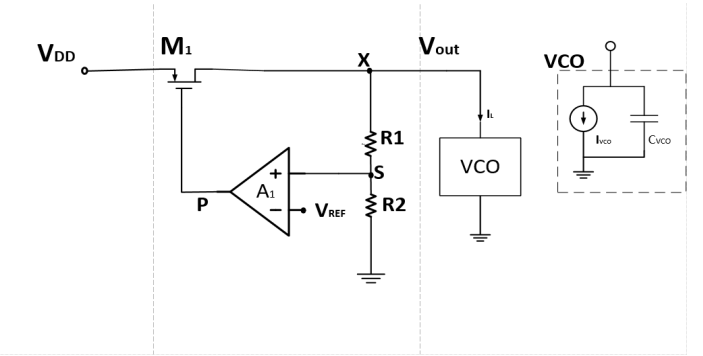

Figure (6): (a) A fundamental LDO structure and (b) model of the VCO.

Design of Op-Amp: -

While designing op-amp a cascode op-amp can be good candidate, in order to achieve the broadest bandwidth for a given gain of the design as discussed, but, keeping in mind of the voltage of low supply, we choose for a straightforward structure of two-stage. We could also proceed with the single-stage Operational Transimpedance Amplifier (OTA), but the problem with the single-stage is that the gain of the amplifier is compatible only with capacitive loads and reduces drastically with resistive loads. So, to achieve higher dc gain we use two-stage op-amp. This circuit has a differential pair. It also employs current-mirror load as a stage, shown in *figure (7)*. To establish the common-mode level at A and B, resistors Ra and Rb fit for that, but nominally load the nodes A and B. This topology escapes cascodes and provides precise bias currents for one and other stages, for example, I_{D5} is replicated from I_{D3}. This way, it thus provides vigorous result. A transistor of technology of 120 nm yields a better voltage gain, and the bigger area of the channel minimizes the flicker noise [6]. The op-amp drags a current of 200 μA [2] from the supply. Now, consider the figure where LDO is interfaced with the VCO. We will now examine the open loop response of op amp A_1. At first, we derive the gain of the op-amp. In two stage op-amp, the gain from input to the terminals A (and B) is given by using the half circuit model as

$$\frac{V_A}{V_{d/2}} = -g_{m1}(r_{o1}||r_{o3}||R_{CM}) \tag{15}$$

So, the fully differential gain is given as

$$\frac{V_B - V_A}{V_d} = g_{m1}(r_{o1}||r_{o3}||R_{CM}) \tag{16}$$

From A (and B) to P, the dc gain is given by approximately

$$\frac{V_P}{V_d} = g_{m1}(r_{o1}||r_{o3}||R_{CM}).\, g_{m6}(r_{o6}||r_{o8}). \tag{17}$$

Here, V_d is the differential input applied to the op-amp's input terminals. Of course, the positive terminal is one where feedback is applied. Here, $Ra = Rb = Rcm = 40\ k\Omega$. Equation (17) is nothing but A_0 in (12). The response of op-amp is shown in *figure (8)*. Here, the curve, starting from 70 dB, is magnitude curve and that of the curve starting from 0 dB is phase curve. We can see that this op-amp provides a gain of up to 40 dB at 110 MHz. Since from the plot op-amp has very poor stability, so we need to stabilize it first as it alone deteriorates the response. Our main objective at this instant is what we called as compensation of the op amp, to achieve a state for a better phase margin (PM). The pole, which is dominant, at node P should be minimized to achieve stability. This can be

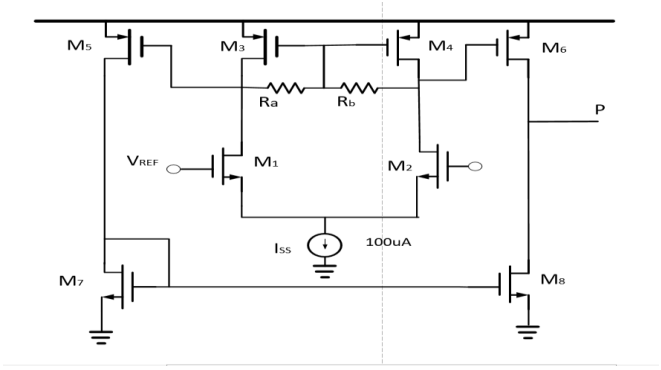

Figure (7): LDO's two-stage op amp.

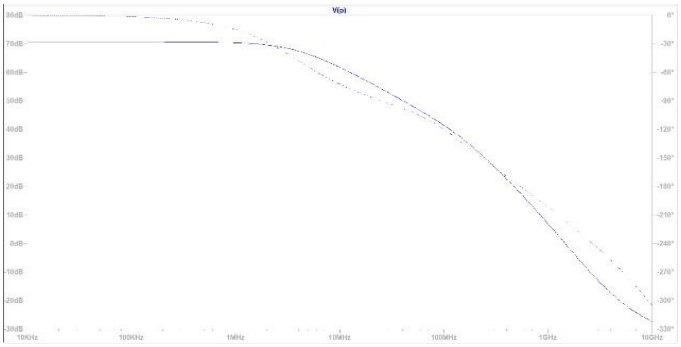

Figure (8): Frequency response of the op-amp.

accomplished by introducing compensation capacitor, Cc = 1pF, both, demonstrates a dominant pole at P, which decides the bandwidth of the system, and leads to pole splitting. This means that the numerical value of the pole at node X has increased to around g_{m0}/C_{VCO} [2]. We also include Rc so as to bring in a zero that wipes out the initial non-dominant pole, because avoiding zero introduction, will lead to a non-minimum phase system and so distract stability. The new frequency response is shown in *figure (9)*, manifesting a better magnitude and phase response. Here, $Rc = 500\ \Omega$.

The circuit in the *figure (10)* is the LDO, having input as V_{DD} and output at V_{out}. The circuit and frequency response of PSRR of closed-loop system is shown in *figure (10)* and *figure (11)* respectively. From the plot we discover that the LDO preserves a rejection ratio of no less than 40 dB about 20 MHz. Now, the output noise [2] voltage of the LDO should not go beyond $25\text{nV}/\sqrt{\text{Hz}}$ at 1 MHz. We observe that the noise is almost as required shown in the *figure (12)*.

We can also conclude that phase margin of the op-amp without compensation and that of the compensated op-amp has huge difference with respect to the stability point of view. The phase margin was very poor in uncompensated op-amp and was unstable, but here compensation of the op-amp leads to stabilization of the op-amp and overall system. We can also draw conclusion that the graph of PSRR is as per the equation (12). The plot of load regulation is also same as that of PSRR but with a division of g_{m0}, that is, the transconductance of pass transistor M_0. We also terminate the discussion that LDO preserves a PSRR of 40 dB up to 21 MHz.

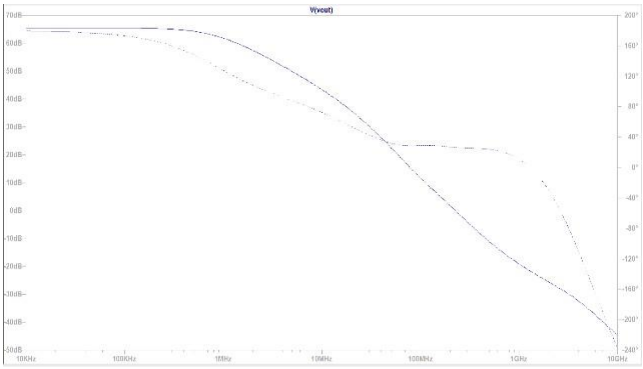

Figure (9): Frequency response of the compensated loop gain.

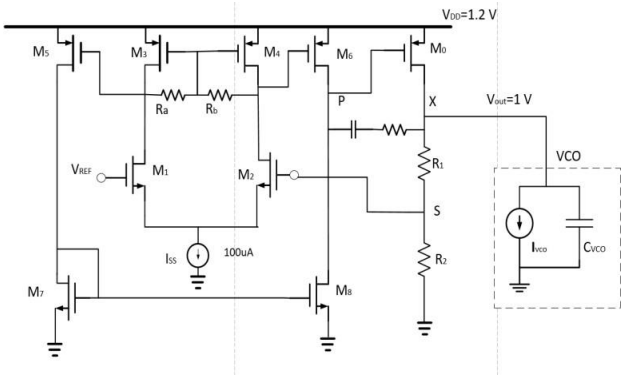

Figure (10): The actual promised LDO circuit.

The peaking in the noise response of the LDO above 110 MHz is due to the fact that there are a number of other components which add up and result in the spectrum. Also, we observe that that noise performance of our design is within the desired range and does not much affect the LDO's performance.

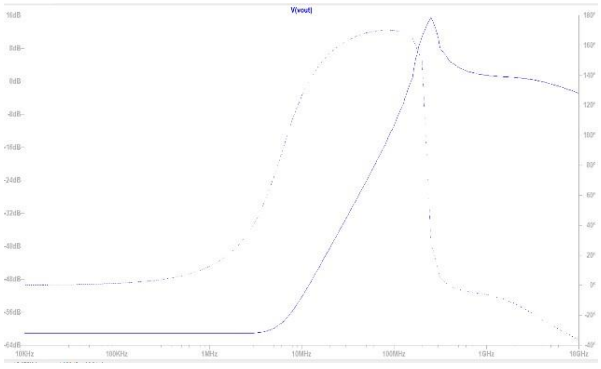

Figure (11): The LDO PSRR versus frequency.

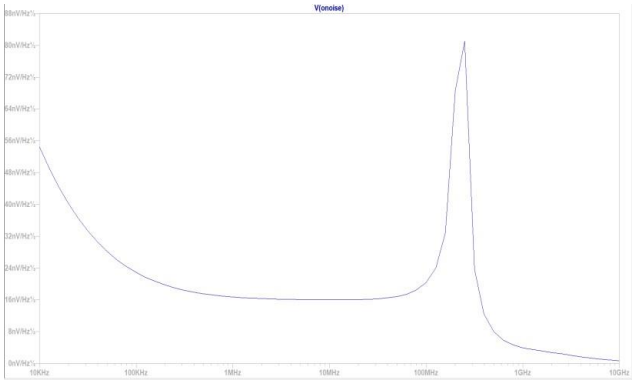

Figure (12): The output noise spectrum of the LDO.

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