# Analysis of IR Drop for Robust Power Grid of Semiconductor Chip Design: A Review

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**Abstract.** Modern semiconductor industry has a major focus on die size reduction and favours the usage of multiple metal layers to increase gross margins. High congestion and voltage or IR drop challenges result from designs with higher and lower core utilisations. Owing to this issue, one of the major difficulties in large silicon-on-chip (SoC) design is the implementation of a power grid design. It's essential to correctly analyze IR drops to guarantee the reliability of the power grid. This paper presents a comprehensive review approach for the analysis of IR drop for robust power grid design in semiconductor chips. The necessity of the vector-based dynamic analysis and the drawbacks of the vector-less analysis have been addressed. The various techniques used to mitigate IR drop effects, including power grid modeling techniques, use of decoupling capacitors, and voltage drop analysis are explored. The review concludes by identifying the most promising techniques for robust power grid design in semiconductor chips and providing recommendations for future research. The simulations are carried out using ANSYS RedHawk, and the analysis findings are achieved using FinFET technology.

## 1 Introduction

Recent years have witnessed much research interest in the analysis of IR drops in the VLSI power grid. Circuit speed may be impacted by IR drops, and in the worst case, these may lead to expensive functional errors. System operability circumstances can be optimised if how the chip's power efficiency is impacted by the IR drop of a power distribution network (PDN) is known. It enables early detection and correction of IR drop effects on a silicon device during design phases. In the past, metal routing and silicon-level power switching circuits were the only factors taken into account in static and dynamic IR drop analyses for silicon chips. Without considering the effects of network elements into account, using this analysis method it is implied that, the power supply from the voltage regulator module to the silicon pads is steady and noise-free. [1]. Although bridge-chip-based interconnect systems provide PDN hurdles, including with the PDN within the bridge of chip can drastically minimize its effect, based on the power map. Power and ground network DC IR drop can be decreased by including ground network in the bridge, power and ground network in the

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bridge chip, and metal-insulator-metal decoupled capacitance in the bridge chip [2]. The international technological roadmap for semiconductors, also known as ITRS, is encouraging the use of carbon nanomaterials in place of traditional copper (Cu) interconnects to address the durability and reliability issues that Cu presents for next-generation on-chip interconnects [3]. For design sign-off, Analysis of dynamic IR drop must be executed precisely. Analysis of the static IR drop, which is an average voltage drop, was useful for sign-off analysis in earlier technology nodes. During the real operation of a chip, it does not take into account an instantaneous high power density. For chip tape-out, which can be crucial to achieve the performance of dynamic IR drop with a variety of real-world conditions [4].

The most crucial stage in the design process is the modeling and verification of the power grid, which is also one of the important technological challenges. The power grid analysis is typically used to complete verification. The modeling procedure is long and extremely complex because the power grid's description spans the entire die area. These are the effects of the requirement to consider many power grid characteristics (non-ideal RLC) along with all devices that dissipate current from this grid is represented in figure 1. Given the resource requirements, it may not be realistic for VLSI circuits to simulate the entire power grid [5]. When the designed circuit consumes more current than the power available, the power supply cannot keep up, resulting in a voltage drop (IR drop) and a reduction in circuit performance. A common signal integrity problem in very deep submicron technology is IR drop. Due to decreasing supply voltage and reduced circuit noise margins, the IR drop not only causes circuit delay but also compromises dependability. The unanticipated peak current consumption ($I_{peak}$), which exceeds the original design's specifications, causes the IR drop [6]. If $I_{peak}$ happens quickly, and at the same moment there is a significant IR drop. However, it is a difficult task to effectively analyse the IR drops due to the physical size of the power distribution network and numerous global interactions between the loads. A conductance matrix that models the impedance of the power grid can be used to define the IR drop analysis procedure as a linear system [7]. Although the IR drop analysis process is simple to formulate, a solution of this linear system is impractical for a typical power distribution network due to its large size. This means that if there are N rows and N columns in the power distribution system, there are $N^2$ total nodes, and the resultant conductance matrix for this power distribution network is $N^2 * N^2$ [8]. It is necessary to predict and minimize IR drop throughout the design process, from placement through signoff, in order to meet IR drop limitations. Additionally, it might be measured after silicon verification. Hence using machine learning techniques, a new method for estimating IR drop during chip design is reported [9] and the traditional approach of using simulation-based commercial tools is too time-consuming and may not be accurate. This method uses a neural network to estimate IR drop, which can significantly reduce the time required for estimation and can provide accurate results even with limited data, making it suitable for early-stage design. Fast estimation of a number of critical chip design metrics, such as design rule violation [10], power [11], crosstalk [12], lithography hotspots [13], testability [14], clock tree's quality [15], placement solution [16], IR drop [17,18], timing and routing solution [19, 20] has become possible. There are numerous ML-based IR drop estimators that target different design stages with different emphases. For predicting timing during the pre-routing phase of chip design using machine learning techniques, the traditional approach of using pessimistic worst-case scenarios can lead to unnecessary design modifications and long design cycles and uses a machine learning model method to predict the timing, which can reduce pessimism and improve accuracy [21]. This paper is categorized by six units. Data files and programme structure and Power grid modeling techniques are described in section 2 and 3. The methodologies and review approaches for IR drop analysis are presented in section 4.

Performance analysis is displayed in section 5. Conclusions are provided in section 6, which also presents the future scope of work.

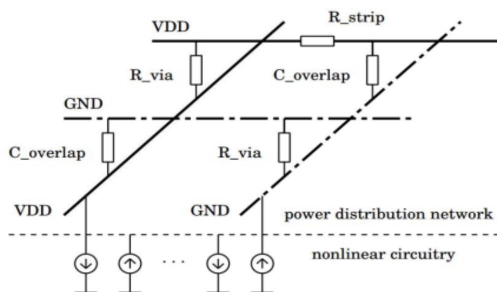



**Fig. 1.** The basic model of the VLSI chip power grid [5].

## 2 Data files and program structure

The focus of work is on the IR drop analysis with report files in a VLSI circuit design using the Ansys Redhawk tool in the top database chip design [22]. Major report files from the analysis tool are enlisted below:

### 2.1 Summary files for power

- *power_summary.rpt:* This file includes a detailed power analysis in each block of chip.
- *power.rpt:* After power calculation this file contains an information of power for each instance.

### 3.2 Static and Dynamic voltage drop result files.

- *dvd file:* This file captures the voltage drop for each instance as the VDD-VSS differential.
- *ir.worst file:* This file details, in decreasing order, the location of the worst dynamic voltage drop (VDD-VSS). The report includes information on the domain name, x-y location, layer name, actual voltage, and ideal voltage.

### 2.3 Static EM and IR drop result files

- *Ir.worst file:* This file lists, in decreasing order, the nodes with the worst static IR drop (VDD-VSS).
- *ins.worst file:* This file lists, in decreasing order, the instances with the worst static IR drop (VDD-VSS). The inst vdd, vdd drop, gnd bounce, ideal vdd, domain name, x y location, and inst name are all included in the report.
- *em.worst file:* In decreasing order, this file lists the worst EM violations for vias and wire pieces. The metal layer, location, EM ratio, domain name, and metal width are all captured in this report.
- *switch_static.rpt:* This file contains information on the voltage and current for the header/footer switches. Only instances of header/footer switches used in low-power design applications are included in this file

## 3 Power grid modeling techniques

The accuracy and run-time efficiency trade-off in the necessary analysis affects the modeling of power distribution networks. In order to calculate the IR drop, a purely resistive model of the power distribution network may be acceptable. However, in order to analyze the network with time-varying currents, a more comprehensive model that takes into account the network capacitances, device parasitic capacitances, explicit decoupling capacitors, and the package's inductance is required [23].
As shown in Figure 2, the on-chip power circuits lines are modeled as RLC components. $R_{vcc}$ is defined as the resistance per unit of length (**Ω/m**) and $L_{vcc}$ as inductance per unit of length (H/m) of supply lines. The inductance includes self and mutual inductances. The series resistance and capacitance $R_d$ and $C_d$ are utilised to model the decoupling capacitor which is carried out by the dummy transistors. $I_s$ is the time-varying switching current of devices. $R_s$ and $C_s$ shown in series indicates the ON resistance and load capacitance of device that is connected to the nodes (A-C, B-D, ..) of power grid. Only linear components like R, L, C, and $I_s$ (current sources) are present in the model shown in Figure 2. It implies to us that the large-size microprocessor power network analysis based on the reported model can be carried out faster using a linear circuit simulator [24].

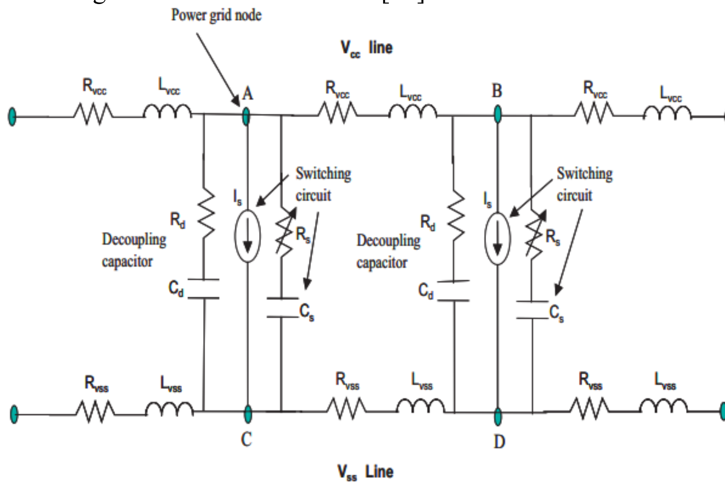



**Fig. 2.** RLC modeling of On-chip power grid

$C_{decap}$ and $R_{decap}$, as illustrated in Figure 3(a), are the two most important decoupling capacitor (dummy transistor) parameters. The charges in $C_{decap}$ are utilised to maintain the voltage supply stability in $C_{sw}$ (switching gate capacitor), before the charges ultimately travel through a sizable current loop between the package to the supply voltage source.

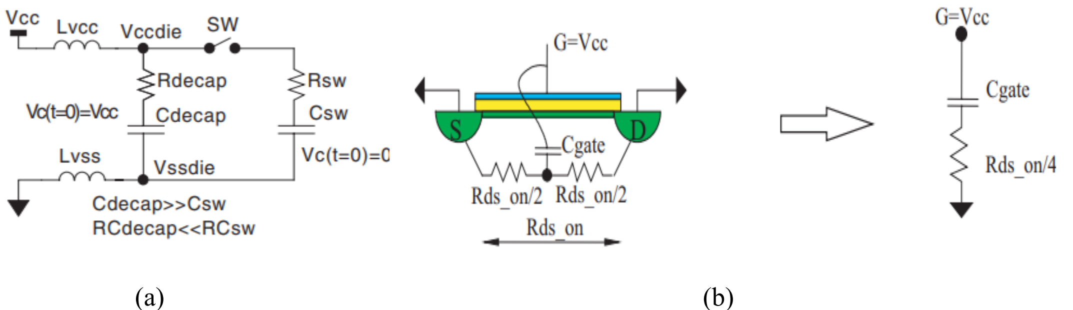



**Fig. 3.** (a) Switching model of the decoupling capacitor and (b) Decoupling capacitor modeling.

It is necessary for the $R_{decap}$ to be suitably small in order to increase the decoupling capacitors' efficiency. As seen in Figure 3(b), an inversion channel between the D and S is produced when $V_{cc}$ is applied to the gate, using the resistance $R_{ds-on}$ . The $I/V$ (current-voltage) graph of the resistor at $V_{ds} = 0$ make up the 1/slope of the $R_{ds-on}$ resistance. A distributed RC network is created by the $R_{ds-on}$ and $C_{gate}$. Figure 3(b) depicts the arrangement of $C_{gate}$ in series with two parallelly connected $R_{ds-on}$ /2 resistors, which adds $R_{ds-on}$ /4 to the series with $C_{gate}$. The accuracy and turnaround time of the power grid modeling are key factors in the power network simulation [24].
Each metal segment can be modeled using either the distributed RC parasitic or the lumped capacitive parasitic, as shown in Figure 4(a), during the RC modeling process. The entire wire capacitance from each driver circuit in the signal net is represented by the lumped capacitive parasitic. The resistance (R) of the metal line is modeled as part of the distributed RC parasitic. Since the metal line resistance of the power grid is important at the full-chip level, power grid modelling typically employs the RC model. Multiple RC segments can be created from a long metal line, as seen in Figure 4(b) [24].

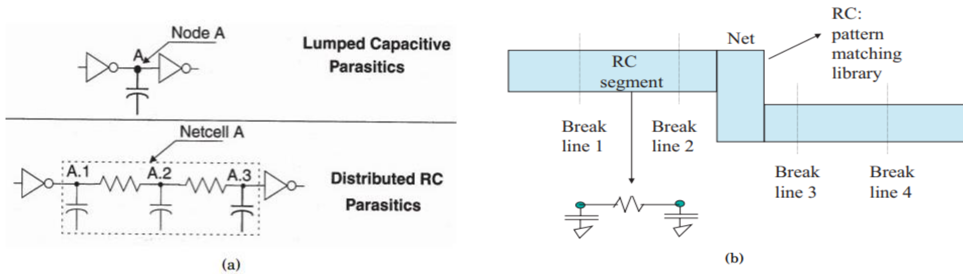



**Fig. 4.** Distributed and Lumped RC models.

Two capacitors are placed at the ends of each series resistor, along with a series resistor, to model each RC segment. Two capacitors uniformly distribute the capacitance of the metal segment. Since it appears to be the representation for pi (π), as seen in Figure 4(b), this model is commonly referred to as the Pi-RC model [24].

## 4 Methodology from IR drop perspective

A reduction in supply voltage known as the IR drop occurs in integrated circuits in power supply networks. As per Ohm's law the resistance of supply rail R, must be proportionate with the supply voltage since the drop is

$$V = IR \quad (1)$$

With the combination of rising current density and shorter widths of the metal line is responsible for this voltage drop. This leads to a lower-than-desired voltage being provided at the standard cells. As a result, delays may rise when the drop is greater and within the noise margin. In some cases, when the drop exceeds noise margins, they might not even switch. The examination of homogeneous multi-core chips' IR drops (DC) is the main topic of Ref [25]. Three categories of homogeneous cores are recognized. three cores: one with the same power supply network, two with the same network structure but a slightly different equivalent resistance, and three with the same resistance values but a similarly different power structure of the network. The IR drop analysis in all 3 kinds of homogeneous multicore chips is addressed using an updated hierarchical analysis method in this work. The results demonstrated that further speedup is achievable with a greater number of homogenous cores.

Dynamic voltage scaling (DVS), as described in Ref. [26], has the potential to significantly reduce the power overhead in FPGAs, but due to the automation of FPGAs, it can be difficult to implement DVS safely for any proposal. This work suggests a reliable worldwide DVS scheme for FPGAs that is designed to run continuously on each FPGA power-up or on a system production process. The outcome shows that for error-free DVS operation, real-time IR-drop and thermal adjustment are necessary. The software that was built to perform data mining on the Power, voltage drop (IR), and Electromigration analysis report records are detailed in Ref. [27]. The output formats from the data collection include two-level web pages, a quick format for visitors to review tables of the essential information, and graphic map files. To make informed decisions on the architecture of VLSI power distribution networks, this work presents research on data mining programs that analyze and manage massive information from multiple sources into a single form.

The issue of IR voltage drop and electromigration (EM) methodologies in deep submicron approaches is covered in Ref. [28], other techniques for determining whether resistance or current is to held responsible for IR drop in a specific area and for regulating the window of time for instances in large IR drop areas to prevent instantaneous switching. A least width is needed in the current metal layer and in higher metal layers to stop electromigration.

A significant issue with the reliability of the power grid in VLSI is electromigration. The routing of both nets i.e. power and signal nets may become too challenging to complete if the power grid is made EM-immortal, according to a new model for predicting the electromigration (EM) durability of via-arrays and EM trustworthiness of the grid vias. A strategy is suggested for balancing reliability and grid integrity to reduce the overall metal area overhead required to reach the required grid lifecycle underneath power integrity limitations in [29]. To accurately analyze an IR drop, in contrast to the two methodologies, the IR-drop analysis takes into account chip heating and packaging self-heating. In this reference, of the major accomplishments is that low-power mobile IC packages accurately measure self-heating caused by current flowing in the trace and the influence of leaking power and self-healing is taken into account to model IR-drop and thermal performance more accurately. Self-heating and temperature-dependent leakage power are taken into account while presenting co-simulation flow for electro-thermal performance evaluation. The thermal effect owing to leakage power and self-healing can have an effect of over 15% on the results of the IR-drop analysis [30]. Issues comes due to IR drop in the extreme performance circuits are analysed. The procedure is made simpler and more effective by the usage of flexible mesh. It is discovered that both the copper surfaces and the vias connection of the voltage regulator module (VRM) cause significant IR drops. The resistance generated through contact of the voltage regulator module and copper planes can be greatly reduced by using a revolutionary technique for IR drop mitigation [31].

The non-ideal components that contribute to the IR drop, which may be static or dynamic, are the resistance within the main power supply and grounded supply lines as well as the capacitance between them. Dynamic voltage drop has an RC transient nature and takes current waveforms inside clock cycles into consideration, whereas static voltage drop merely takes average currents into consideration. Similar effects, known as ground bounce, can be observed in ground wiring. Both of these impacts result in lower operating voltages for devices. This in turn lengthens the total time response of a device and may result in a failure. The Ldi/dt noise is brought due to induction coupling, occurred due to sudden voltage changes in the wire of grids and changes in wire is caused by current spikes in the voltage rails [32]. Average voltage drop for the design is known as static IR drop. In earlier technology nodes with adequate built-in capacitance for decoupling from the power distribution network and non-switching circuitry, static IR drop was useful for sign-off

analysis. In contrast, dynamic IR drop evaluates the IR drop brought on when numerous circuits switch simultaneously, establishing a peak current demand, and the reliability and performance of the chip are directly impacted by the strength of the power grid. Therefore, multiple iterations of the power-grid analysis are required during the design phase of the process. [33,34]. To perform the static and dynamic analyses, a running Redhawk flow is shown in Figure 5.

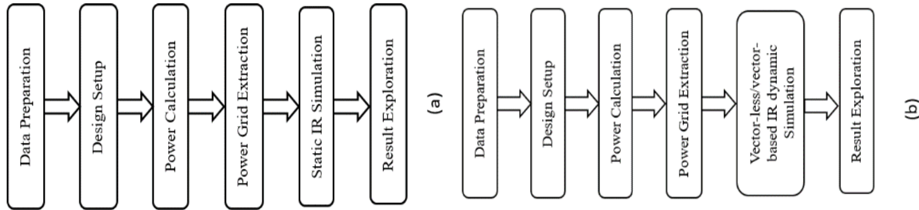



**Fig. 5.** A flow of IR drop analysis (a) Static IR analysis (b) Dynamic IR analysis.

## 5 Performance analysis

### 5.1 Vector-less dynamic IR analysis

There are two different ways to perform a dynamic IR drop analysis. The first analysis known as vector less and the other is a vector-based analysis. Moreover, In the second approach of IR drop analysis both the files, VCD (Value Change Dump) and DB (Data-Base) is importable. In our illustration, a vector of the VCD type was used in each simulation. The VCD contains data on many use-case situations that encompass various switching activities. The vector-based analysis is suggested for reliable analysis. Because the average chip power is directly applied in vector less analysis or perhaps a toggling rate related to the typical chip power is directly applied. The stated average power may or may not be appropriate for a dynamic IR drop study, unfortunately. Depending on when average power is calculated or monitored when the chip is functioning, the average power can vary significantly. Often, the entire use case scenario is taken into account when determining the power requirements of a semiconductor. Thus, using the average power that is now provided is unacceptable. There is a way of overcoming the issue of using the average power as it is by using two to three times the average power. Yet, the area of a hotspot increases with the amount of power delivered. Vector-less dynamic IR drop analysis performs too many iterations during the last stages of execution to meet the IR drop sign-off.

### 5.2 Vector-based dynamic analysis

The output of the true-timing gate-level modeling, also known as gate to VCD (gate-level VCD), can be used to produce an analysis of IR drop exceptionally specific for dynamic drops. The generation and simulation data of gate-level with true-timing, however, frequently takes an unnecessarily long period of time and is frequently delayed until the conclusion of the design cycle. Hence, zero delay Gate-VCD (GVCD) or RTL-Verilog simulation analysis (RTL-VCD) can be used. Calculated toggling rates are then propagated to logic utilizing state propagation from the RTL-VD for the main primary inputs and registers output such as flop/latch and then utilizing state propagation, this activity is transmitted to logics.

Unfortunately, there is frequently a name mapping problem from RTL to gate level. Moreover, it is less effective than analysis done with a gate-VCD. As a result, gate-VCD from a synthesis netlist is employed to simulate the dynamic IR drop sign-off in the minimal transistor level simulation. Moreover, a wide range of realistic switching scenarios and extensive analysis coverage is crucial for gate-VCD. Hence four different gate-VCD types from different CPU benchmarks are used for the simulation [4]. Using ANSYS Redhawk, simulations were carried out.

In order to take in to consideration the peak current consumption for the IR drop brought on by the chip's actual functioning as well as the instantaneous switching of instances, vector-based analysis is required. One of the two instances is switched when analysis coverage reaches 50%. As a result, the more correctly the IR Drop analysis can be evaluated, the closer the analysis coverage is up to 50%. And analysis coverage is indicated by the ratio of the number of switching instance to total number of instances, as given in eq. (2) [4]. But if two instances cluster each other and switches at the same time causes more IR drop issue as we can see in Figure 6.

$$Analysis\ coverage\ (\%) = \frac{No.\ of\ switching\ instances}{No.\ of\ total\ instances} \times 100 \quad (2)$$

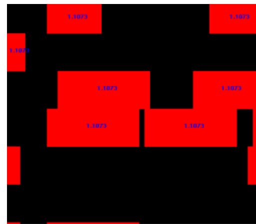
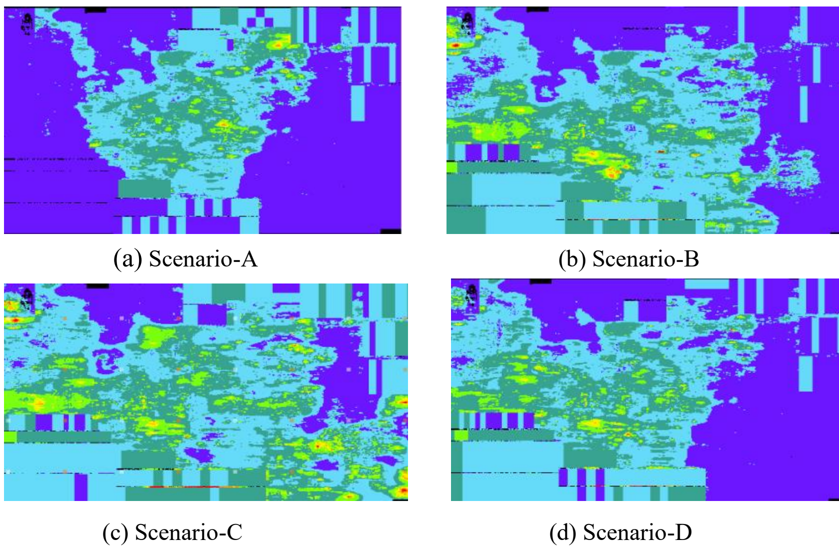


**Fig. 6.** A case of worst instances.



(a) Scenario-A (b) Scenario-B

(c) Scenario-C (d) Scenario-D

**Fig. 7.** Maps of dynamic IR drop with four different scenarios [4].

Figure 7 displays dynamic IR drop mappings for each gate-VCD. Table 1 provides the analysis coverage for each situation of the scenario as well as the overall analysis coverage for all scenarios considered. for scenario A the analysis coverage is 18%, which is the least value. However, by utilizing different scenarios, the analysis coverage can be raised to over 43%. Thus, it is crucial to improve analysis coverage in addition to using genuine operation scenarios with gate-VCD. If there are many instances that the scenario being used does not cover, then either another scenario is needed, or vector-less analysis with switch rate must be added.

**Table 1.** Analysis of coverage.

| Scenario-A | Scenario-B | Scenario-C | Scenario-D | All Scenario |
|---|---|---|---|---|
| 18.1% | 31.4% | 19.3% | 19.4% | 43.4% |

### 5.3 IR drop mitigation

***5.3.1 Cell padding for clocks:*** When it comes to IR drop concerns, Clock design is the primary cause of the chip's excessive power consumption owing to clock switching. Therefore, using the padding clock cells methodology, the insertion of standard cells and any excessive cell density close to the clock buffers/inverters and clock gate cells is avoided. This reduces the chance of a dynamic IR drop.

***5.3.2 High IR drop instances require current and resistance:*** Examine the differential voltage report, which includes the voltage present in the designs' standard cell instances. By loading the respective state directories, individually the resistance reports for $V_{DD}$ and $V_{SS}$ are generated. Thus, the steps involved are :

- Take appropriate value of resistance from given report files of resistance.
- To calculate the total resistance, sum up all the resistances.
- To calculate the voltage drop, instance voltage is subtracted from the supply VDD.
- Add together all the resistance and divide by voltage drop.

***5.3.3 IR drop with surrounding cells:*** It can be determined whether an IR drop is caused by resistance or by the high current demands of cells with high drive strengths if we are aware of the cells that surround the drop location. If the cells in the vicinity of the IR drop regime have a larger drive strength, then current is responsible for the drop, if the standard cells are of normal driving strength, supply rail resistance is responsible for drop. The following steps are involved to analyze high IR drop instances with surrounding cell.

- Obtain a sample from the file that the script generated in order to calculate the current caused due to drop.
- Determine the coordinates of instances and increase the x-coordinates by 10um,
- Double the row height and add it to the y-coordinates.
- Verify to see if these new coordinates cross tile boundary lines.
- Assign the new coordinates to the relevant tile coordinate if they are intersecting.
- Query for instances there.

***5.3.4 De-cap insertion:*** Make a de-cap around the dynamic IR hotspot zone.

## 6 Conclusion and Further scope of work

Robust power grid analysis is made achievable by the analysis methods described in this paper. The analysis coverage of the main scenarios for the vector-based dynamic IR drop

simulation model is reported. To increase estimation accuracy, a methodology is described for IR drop analysis in power estimating at various designing phases. The traditional lumped RC model is a simple and efficient technique for analyzing power grids, but it lacks accuracy in modeling complex structures and dynamic voltage drop effects. The distributed RC model offers higher accuracy but at the expense of increased computation time and complexity. The electromagnetic simulation-based techniques, such as the finite element method and method of moments, provide even higher accuracy and are suitable for analyzing complex power grid structures and high-frequency effects. However, these techniques also require significant computational resources and may not be suitable for large-scale designs. The promising future techniques for power grid modeling include machine learning-based approaches, which have the potential to significantly reduce simulation time while maintaining accuracy. Other emerging techniques such as circuit-level simulation and hybrid approaches combining different modeling techniques also offer potential advantages for power grid analysis.

To summarize, IR drop evaluation is an essential part of VLSI design that promotes the functionality and dependability of integrated circuits. It is essential to accurately estimate the voltage drop and optimize the design parameters to reduce its effects utilizing various tools and methodologies. But still, IR drop analysis is a challenging operation that necessitates a thorough comprehension of the physical characteristics of the circuit as well as proficiency with the analysis tools. To ensure a successful VLSI design, it is crucial to stay abreast with the newest processes and techniques. Understanding the effects of dynamic IR on the timing action of the device, including path mode and timing productivity, is the main focus of this research. Covering of the various scenarios without requiring replicating each one separately though difficult is another topic of research. Moreover, the impact of dynamic IR on trial methods shall be further studied. To build a strong connection between analysis and actual device functioning, efforts are being made to integrate analysis and semiconductor measurements.

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