Design and Performance Optimization of Split Capacitor Digital-to-Analog Converter(DAC) for SAR-ADCs

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Abstract. This paper presents two novel digital-to-analog converter (DAC) designs that leverage the split capacitor approach. The designs optimize speed, and accuracy, significantly improving linearity and overall performance. Integrating a binary-to-thermometer code (B-TC) decoder at the switching network of the split capacitor techniques further enhances the performance of DACs in terms of linearity, and speed. Also, it reduces the capacitive mismatch associated with capacitive DAC designs. Using Cadence Virtuoso UMC 180nm technology, the designs were implemented with a 90fF capacitance value at 1.8V supply voltage. The performance of these proposed DAC configurations, one with a B-TC decoder and another without is assessed through simulation to benchmark them against state-of-the art designs. According to simulation results, the DAC with an integrated B-TC decoder performs significantly better, which makes it ideal for SAR-ADC design applications that need high speed, low power consumption, and area efficiency.

1 Introduction

Modern electronic systems need digital signals for their effective processing and information storage. The analog signals from the physical world must be converted into digital (binary values “1” or “0”) for signal processing in digital domain and back to analog for human understanding. This conversion process is carried out by analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) respectively [1]-[2]. Analog circuits can perform simple tasks effectively like filtering and amplification, but not suitable for complex computations because of their limitations with respect to analog signals [3]. Such complex problems are addressed in digital domain by using digital signal processing (DSP) techniques after signal conversion from analog to digital form. DSP also helps to enhance capabilities of system by storing data accurately and providing a high signal-to-noise ratio (SNR) [3]. The recent technology advancements including machine learning (ML), artificial intelligence (AI), along with digital computers further

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streamline the processes, causing the importance of data conversion in contemporary electronic systems. ADCs performance determines the speed and efficiency of these systems [4]-[6].

Therefore, data converters are crucial components in the signal chain of modern communication systems and are widely used in system-on-chip (SoC) design to integrate several functionalities [7]. However, the performance of the system is improved by integrating the ADCs and digital backend into a single chip. Successive approximation register (SAR)-ADCs have become well-known among ADCs designs because of their better power efficiency and CMOS technology scalability. However, at high conversion rates (>100MS/s), their efficiency degrades due to process limitations [8]. The design of a split capacitor digital-to-analog converter (DAC) for high-speed SAR-ADCs is investigated in this work. The emphasis made on DAC design is to improve accuracy, speed, and reduce power consumption with reasonable real estate [9]. Figure 1 shows the flowchart of the data conversion process for analog-to-digital and vice versa.

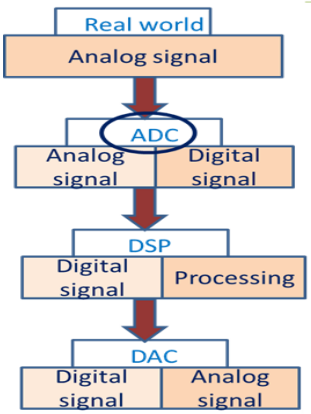

Figure 1. Data conversion process of A/D and D/A

This paper provides the design and performance optimization of a novel DAC for the enhancement of SAR-ADC overall performance. The background of DAC is presented in Section II, and the suggested DAC design and analysis are presented in Section III. The simulation results and a comparison of the suggested design with other potential designs are covered in Section IV. Section V winds up the paper.

2 Back Ground

Figure 2 shows the block diagram of SAR-ADC, which consists of three important blocks comparator, D/A converter, and digital control logic. The DAC is a crucial block, whose output is driving one of the inputs of the comparator with generated reference voltage for comparison. The collective signals from digital logic control drive as an input to DAC through a switching network made up of using either a resistive ladder (R-2R) or a capacitive ladder (C-2C). The DAC-produced reference voltage allows the performing of binary search operations in SAR-ADCs.

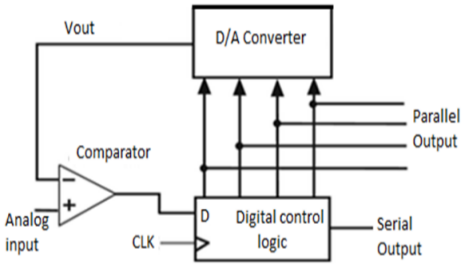

Figure 2. SAR-ADC block diagram

2.1 Resistive R-2R DAC

The DAC contains a switching network at the input section made up of using resistive R-2R ladder.

- The resistive R-2R ladder is commonly used in the switching network of DAC for low to medium applications due to its ease of use and scalability [1].
- It is a binary-weighted resistor network, with resistor values alternating between R and 2R.
- The network produces an equivalent analog output by using digital logic control to generate digital signals.
- The design can be easily scaled to accommodate higher resolutions without significant changes to the resistor values.

$$V_{out} = V_{ref} \cdot \frac{D}{2^N} \qquad (1)$$

Where V_{ref} is the switching network generated voltage, D is the input digital value, and N is the number of digital input bits.

The R-2R DAC has several shortcomings:

- Non-linearity at higher resolutions due to mismatch errors from resistor manufacturing variations [10].
- Power inefficiency because it requires constant current flow, which reduces efficiency in power-constrained systems [7].
- Speed limitations due to the RC time constant, making it unsuitable for high-speed ADCs [11].
- An alternative approach to mitigate these issues is the C-2C switching network in DAC designs [12].

2.2 Capacitive C-2C DAC

The switching network of the resistive R-2R ladder in the DAC was replaced by a capacitor array with values of C and 2C. This configuration is more suitable for modern designs because of its energy efficiency and seamless integration with CMOS technology

[9]. Moreover, this design is preferable for high-density designs with limited real estate [1]. High-speed ADC applications can benefit from reduced parasitic resistance and capacitances of C-2C DACs [10].

However, this architecture is not recommended for high-resolution systems, whose accuracy is prone to capacitor, value mismatch [11]. Furthermore, with the resolution, the design complexity rises because of exponentially growing capacitors, creating a problem of parasitic and stray capacitances [7]. Many researchers have addressed these issues and proposed several methods like split capacitor D/A converter, and segmented D/A Converter, to enhance the DACs performance to increase accuracy and efficiency [12]– [14]. However, despite advancements, there is a gap in the DACs' performance, in terms of linearity, speed, area, and power dissipation. Here we propose D/A Converter designs using multi-split capacitor approaches for performance optimization.

3 Proposed DAC Architectures

The proposed DAC design uses three attenuation capacitors in its switching capacitive network with the calculated values from equation (2). This technique helps to divide the charge-scaling capacitive D/A capacitor array efficiently, which enables minimizing the total capacitance required and helps in area optimization, and speed improvement.

3.1 Advantages of Proposed Designs

3.1.1 Improved Linearity and Accuracy

The suggested multi-split capacitor D/A converter with three attenuation capacitors improves accuracy by limiting both differential nonlinearity (DNL) and integral nonlinearity (INL) because of its low capacitance mismatch.

3.1.2 Compact and Space-Efficient

Because a limited range of capacitor values are incorporated in the switching network, this method is well-suited for applications where silicon area is crucial and optimizes the overall area required.

3.1.3 Enhanced Power Efficiency

The suggested designs are suitable for power-sensitive systems because they consume only dynamic power.

- The three attenuation capacitors help reduce glitch errors at the DAC output during switching operations, ensuring smoother signal processing.
- Small capacitance values allow for quicker charging and discharging times, which enhances the overall conversion speed.

The proposed split capacitor D/A converter is a reliable and optimal solution for modern SAR-ADCs due to its reduced capacitance, improved performance, and operational efficiency.

3.2 Design Procedure

The attenuation capacitance calculated from equation (2):

$$C\_attenuation = \frac{\Sigma\,(LSB\ array\ Capacitors)}{\Sigma\,(MSB\ array\ Capacitors)}.C \qquad (2)$$

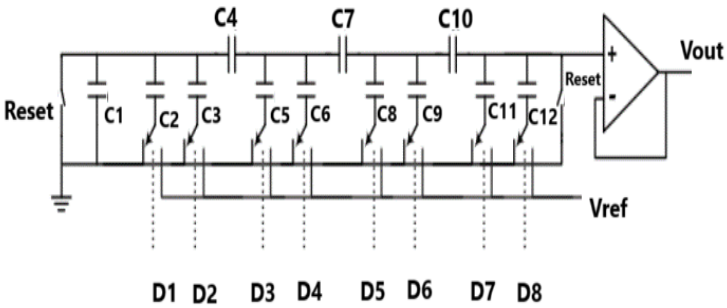

Figure 3. Proposed split capacitor DAC

The proposed configuration, shown in Figure 2, incorporates three attenuation capacitors (C_4, C_7, and C_{10}) to reduce the chip area instead of using a single attenuation capacitor. To calculate the value of each capacitor, we assume a digital input code of D = 10000000. Given that 1LSB = $\frac{V_{ref}}{256}$, this means that the digital input D corresponds to 128LSBs. Consequently, the output voltage of the digital-to-analog converter can be expressed as:

$$V_{Out} = 128.\frac{V_{ref}}{256} = \frac{V_{ref}}{2} \qquad (3)$$

The equivalent capacitance observed from the node opposite to C_{12} should match its value. Therefore, each capacitor's value corresponds to the capacitance seen from the node to the left of the capacitor network. For a digital input code of D = 00000001, switch D_1 is activated, with all other switches off. The equivalent capacitance observed from the node opposite C_{12} should equal its value. Consequently, the capacitance of each capacitor corresponds to the equivalent capacitance measured from the node to the left of the capacitor network. For a digital input code of D=00000001, only switch D_1 is activated, while all other switches remain off. After that,

$$C_2 = C_1 \qquad (4)$$

In an alternative scenario, if the digital input code is D = 00000010, switch D_2 is activated, while all other switches remain off, connecting capacitor C_3 to V_{ref}. This configuration can be expressed as:

$$\frac{C_3}{(C_1+C_2+C_3)}.V_{ref} = \frac{V_{ref}}{2} \quad (5)$$

Equation (5) leads to the conclusion that $C_3 = 2C_1$. The voltage $\frac{V_{ref}}{2}$ should be the node voltage across from the capacitor C_5. If C_5=C_1 and the digital input code is D = 00000100. Consequently, capacitor C_4 may be written as:

$$\frac{C_5}{[(C_1+C_2+C_3)\| C_4]+C_5}.V_{ref} = \frac{V_{ref}}{2} \quad (6)$$

Using equations (5) and (6) as references:$C_4 = \frac{4}{3}.C_1$

Assuming C_1=C, the values for all capacitors in the proposed split-array DAC configuration can be derived and the specific values for each capacitor are provided in Table 1. Consequently, the total capacitance in the suggested configuration is computed as follows:

$$C_{total} = C + C + 2C + 3(\frac{4}{3}.C + C + 2C) = 17C \quad (7)$$

The proposed split-capacitor DAC (SC-DAC) switching network can be further optimized by incorporating a 2-bit binary-to-thermometer code (B-TC) decoder. This integration enhances the overall performance of DAC by improving linearity, reducing switching errors, and further minimizing glitch noise during digital-to-analog conversion.

Table 1. Capacitor designed values

Capacitor Name	Value Assigned	Capacitor Name	Value Assigned
C_1	C	C_7	$2C$
C_2	C	C_8	4/3.C
C_3	$2C$	C_9	C
C_4	4/3.C	C_{10}	C
C_5	C	C_{11}	$2C$
C_6	C	C_{12}	4/3.C

3.3 Binary to Thermometer Decoder

Each 2-bit input code of the proposed DAC uses the 2-bit binary to thermometer code decoder, which is depicted in Figure 4. The truth table is given in Table 2.

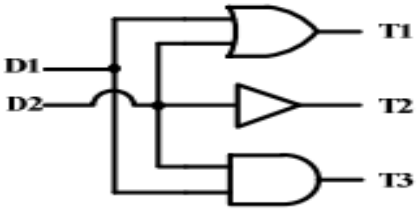

Figure 4. 2-bit B-TC decoder

Table 2. Truth table of 2-bit B-TC decoder

Binary Code		**Thermometer Code**		
D2	**D1**	**T3**	**T2**	**T1**
0	0	0	0	0
0	1	0	0	1
1	0	0	1	1
1	1	1	1	1

Using a 2-bit B-TC decoder enables the circuit to utilize three capacitors of value C, instead of a mix of C and $2C$capacitors. This modification enhances dynamic performance and minimizes capacitor mismatches, limiting discrepancies to only between C and $\frac{4}{3}.C$, instead of differences between C, $2C$, and $\frac{4}{3}.C$.

Furthermore, the highest value of a capacitor is decreased to $\frac{4}{3}.C$ rather than $2C$. This helps decrease the charging and discharging times, improving the speed. A split C-DAC without a B-TC decoder is shown in Figure 5, and a split C-DAC with an integrated 2-bit B-TC decoder is depicted in Figure 6.

3.4 Implementation of Split Capacitor DAC

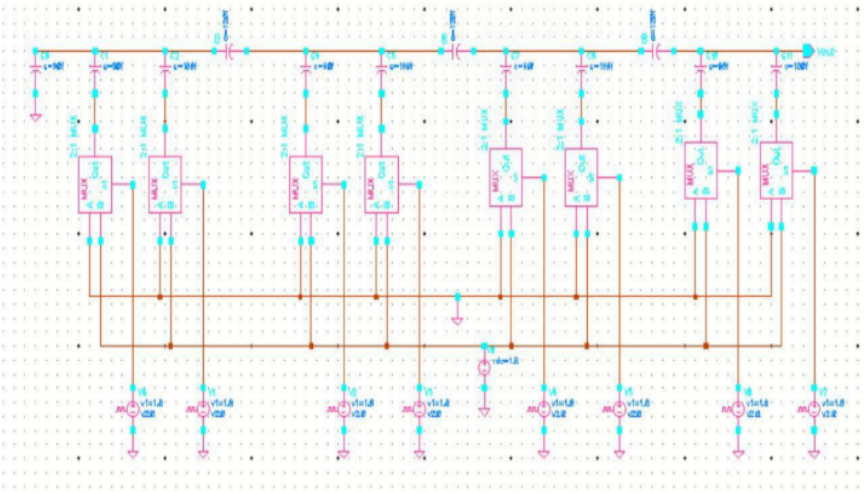

Figure 5. Schematic of split capacitor DAC (SC-DAC)

3.5 Implementation of Split Capacitor DAC with B-TC Decoder

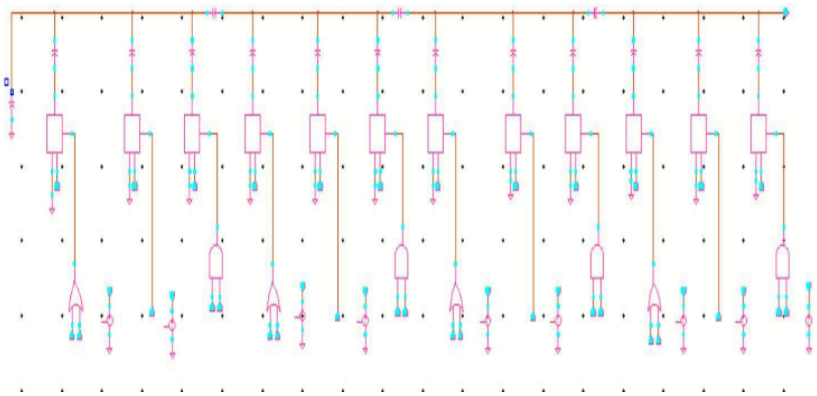

Figure 6. Schematic of split capacitor DAC (SC-DAC) with B-TC decoder

4 Results and Discussion

The simulation was performed using UMC 180nm technology on the Cadence Virtuoso platform, with a supply voltage of 1.8V and a capacitance value of 90fF. The results of the simulation for the proposed Split C-DAC with the binary-to-thermometer (B-TC) decoder are presented in Figure 6. For the sake of brevity, the corresponding simulation results for the configuration without the B-TC decoder are omitted. The purpose of these

simulations was to assess the performance improvements brought by the integration of the B-TC decoder in the DAC design.

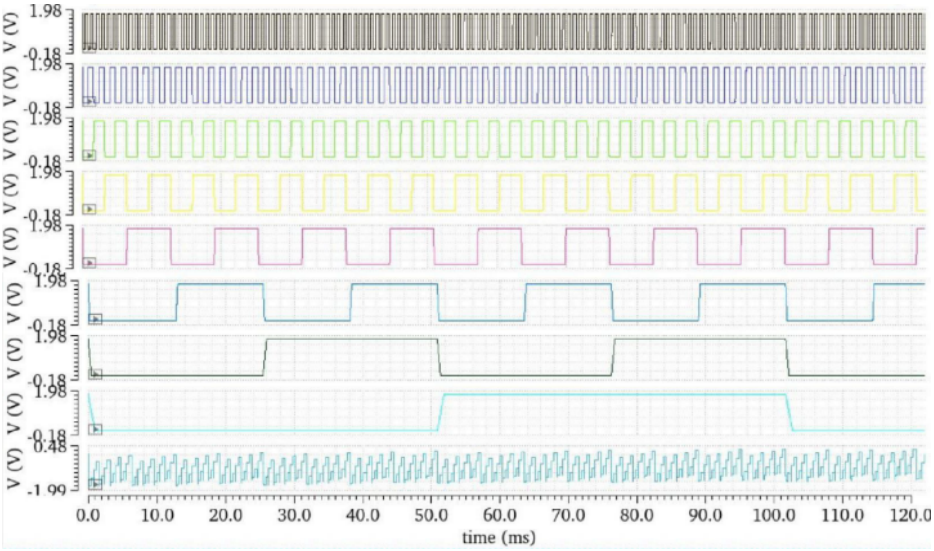

Figure 7. Simulation results of proposed split C-DAC with B-TC decoder

Table 3. Performance comparison

ParameterAttributes	Conventional C-2C DAC	Proposed SC-DAC	SC-DAC with B-TC Décoder
Voltage (V)	1.8	1.8	1.8
Total Capacitance (fF)	2886	1530	1530
Resolution (Bits)	8	8	8
Power Dissipation (μW)	760	764	765
DNL (V)	0.84 LSB	0.256 LSB	0.217 LSB
INL (V)	1.34 LSB	0.613 LSB	0.472 LSB

5 Conclusion

We designed and simulated two innovative split capacitor array DACs using Cadence UMC 180nm technology with a capacitor value of 90fF. The switching network is optimized by dividing the capacitive array into three segments with three attenuation capacitors, effectively reducing capacitor sizes and improving precision. The proposed SC-DAC and SC-DAC with B-TC Decoder outperform conventional C-DAC designs, achieving a 53% reduction in area. Figure 4 employs three small capacitors with values C, $2C$, and $\frac{4}{3}.C$, while Figure 5 further simplifies the design by using only C and $\frac{4}{3}.C$. This approach minimizes capacitance mismatches and effectively reduces nonlinearities.

As shown in Table 3, the proposed SC-DACs require a total capacitance of only 1530fF for an 8-bit DAC, achieving a 47% reduction as compared to conventional split capacitor DAC. While power dissipation is nearly identical across all designs, the proposed designs demonstrate significant improvements in linearity. The SC-DAC reduces DNL by 69.05% (to 0.256 LSB) and INL by 54.37% (to 0.613 LSB) compared to the conventional C-$2C$DAC. Adding the B-TC Decoder to SC-DAC further enhances performance, reducing DNL by an additional 15.23% (to 0.217LSB) and INL by 23.01% (to 0.472LSB). Therefore, the proposed SC-DAC and SC-DAC with B-TC Decoder offer up to 69% improvement in DNL and 54% in INL, while maintaining comparable power consumption. These features make them highly suitable for high-precision, area-efficient, and high-speed applications in SAR-ADC Designs.

References

1. B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill Education, 2018.
2. D. Johns and K. Martin, Analog Integrated Circuit Design, 2nd ed., Wiley, 2012.
3. A. Sedra and K. C. Smith, Microelectronic Circuits, Oxford University Press, 2020.
4. S. K. Mitra, Digital Signal Processing: A Computer-Based Approach, McGraw-Hill Education, 2010.
5. J. G. Proakis and D. G. Manolakis, Digital Signal Processing: Principles, Algorithms, and Applications, Pearson, 2007.
6. B. Murmann, "ADC Performance Survey 1997–2023," Online Database.
7. Murmann, B. "The Race for the Extra Decibel: A Brief Review of ADC Performance Evolution." IEEE Solid-State Circuits Magazine, 2020.
8. C. C. Lee and M. P. Flynn, "A SAR-Assisted Two-Stage Pipeline ADC," in IEEE Journal of Solid-State Circuits, vol. 46, no. 4, pp. 859-869, April 2011, doi: 10.1109/JSSC.2011.2108133.
9. Wang et al. "Split Capacitor Architectures for High-Speed SAR ADCs." IEEE Transactions on Circuits and Systems, 2021.
10. Chen, R., et al. "Calibration Techniques for Mismatch Error in Capacitive DACs." IEEE Transactions on Circuits and Systems-II: Express Briefs, 2020.
11. Pan, Y., et al. "Analysis and Design of High-Speed SAR ADCs with Hybrid DAC Architectures." IEEE Journal of Solid-State Circuits, 2019.
12. MasoudNazari, Armin Aghajani and Omid Hashemipour “Design of a new split-capacitive-array DAC based on distribution of attenuation capacitor” in 2015 23rd Iranian Conference on Electrical Engineering (ICEE).
13. Savitha.M R., Venkat Siva Reddy, “A 14-bit Dual-Split Capacitor Array DAC Design Based Successive Approximation ADC” in International Journal of Recent Technology and Engineering (IJRTE) ISSN: 2277-3878, Volume-8, Issue-1, May 2019.
14. Y. Li and Y. Lian , “Improved binary-weighted split-capacitive array DAC for high-resolution SAR ADCs” in ELECTRONICS LETTERS 14th August 2014 Vol. 50 No. 17 pp. 1194–1195.