Design of Free Space Optical Communication for Efficient Communication

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Abstract. Free Space Optics is a form of Optical Wireless communication technique that uses free space as a medium between transmitter and receveur. It is especially useful for short range point-to-point communication links when a physical communication connections is not economical and feasible. In light of the benefits a FSO can offer, there has been a significant increase of interest in research community to develop efficient FSO transmitter and receveur system. This work is focused on the développent of efficient communication link for optical sources with very low Pulse-Répétition-Frequency. The main contribution of this work is the développent of simple yet efficient alternatives to the traditional topics of FSO design like PPM Modulation, Synchronisation etc.

1 Introduction

Free Space Optical Communication

Free space Optics (FSO) is an optical communication technique that uses light propagation th rough free space, namely vacuum, outer space, air etc, to transmit data Wireless. This méthode of communication is in contrast to the two traditionnel methods mentioned below

1. Wireless – RF Communication

2. Optical Fiber Communication(OFC)

RF based communication uses electrical data signals modulated by RF frequency electro-magnetic waves and sent across the medium through antennas. There is no optics involved in this method. It is the choice of communication for cellular devices, mobile networks, wireless networks etc

Although FSO is similar to OFC, the main difference lies in the medium that the light propagates. In OFC light is guided by the walls of the glass fiber, whereas in the FSO, the light is unbounded by the medium and hence the name free space optic High speeds, ase of

deployment,Low BER,Absence of sidelobes,License-free operation Immunity to RF interference,Reduced maintenance costs

FSO Disadvantages, High Attenuation,Beamdispersion Interference from background light sources The above features make FSO the best choice for short-range point to point communication links Components of a FSO system are:Electronic Message Data Generator,A Base band modulator, Driver circuit which controls the opticalsource,Optical Source (Laser orLED),OpticalDetectors, Demodulator

Scope of the Research Work :Designing a complete FSO system is a complicated process in terms of time and effort invested, especially the optical part. In this work, the focus is mainly on the design of the electrical aspects of the system, in such a way that pre-defined specifications of the optical front-end are assumed and the overall requirements from a communication system point of view are met.The main objective of this work is to design an efficient communication link with the below system specifications.

1.1.1: Data rate – 20kbps or more
1.1.2: Bit-Error-Rate (BER) – 10^-6 orbetter
1.1.3: Laser Pulse Repetition Frequency (PRF) –10KHz
The scope of the work is only the design of the electrical aspects of the communication link and the following procedure talk about the design process and its performance evaluation.

2. Transmitter Design

The *process* of arriving at the solution than the solution itself is the prime focus of this chapter.

Any system design starts with the user requirements. Then a thorough scientific investigation is done on the requirements to come up with a feasible solution.

Requirements: Data Rate – 20kbps or more,BER – 10^-6 orbetter, Laser PRF – 10KHz,Pulse Width – 20ns

In order to meet the above requirements, we can think ourselves the below basic questions, the solutions of these will enable us to come up with a complete solution for the system. What modulation scheme to be used to meet the given data rate in a FSO environment? Is any channel coding technique is required to meet the given BER.How will the low laser PRF affect the aboveissues Each one of the above questions is answered separately in the below sections

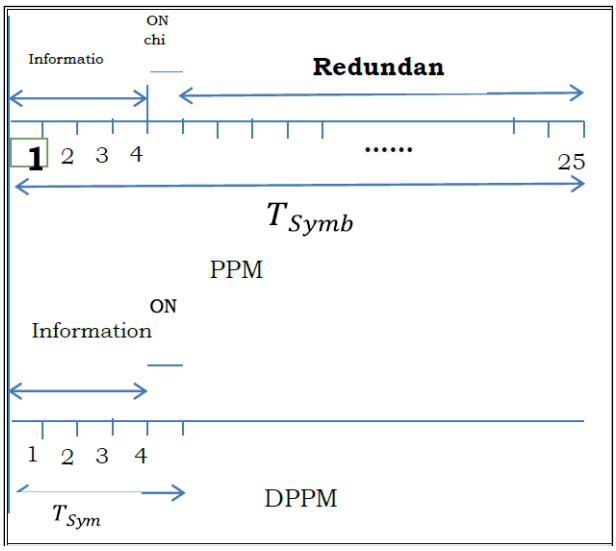

Fig.1: PPM Vs DPPM

Now if we apply the regular PPM for the current requirements (assuming a 256-ary Modulation only for illustration purposes, the choice of optimum number of bits/symbol is discussed in ResultsChapter),Total Symbol time = 256*pulse_width = 256 * 20ns = **5.1us**Data rate = $8/T_{symb}$ = **1.6 Mbps >> 20kbps requirement**From data rate point of view, the simple PPM method performs extremely well.AT_{symb} of 5.1us means, the laser should be capable of emitting two pulses in two PPM symbols duration, i.e. 2*5.1us = 10.2us. But it is clearly not possible as the laser can only emit pulses every 100us (because of Laser PRF of 10 KHz). Hence the simple PPM approach is not applicable to the currentscenario.

Error Control Coding

A forward error correction (FEC) based on convolution coding is presented. It is agreed that channel is prone to errors and the need is felt to accommodate a convolution encoder in the design.
An FEC adds redundancy to the data bits enabling error correction capability at the receiver and thereby improving bit-error-rateperformance.
It is suggested to use a ½ rate convolution encoder with a constraint length equal to 7, as shown in Fig 2. The generator polynomials used to derive its two bits A and B are 133 and 171 (octal)respectively.

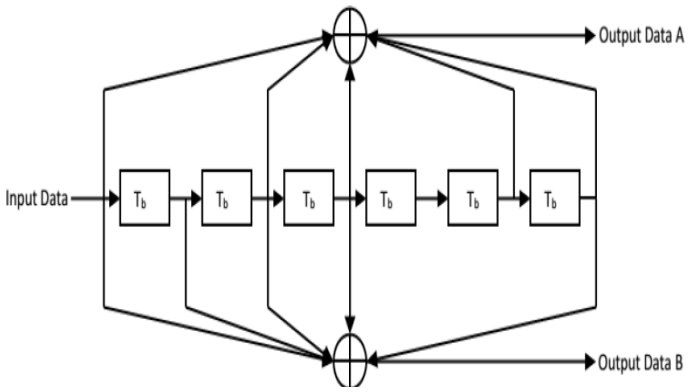

Figure 2: ½ rate Convolutional Encoder

Interleaver

Random burst errors are common in a FSO channel. So, it is suggested to use a simple 4x4 row in, column out interleaver to combat the burst errors.

Data In

1	2	3	4
5	6	7	8
9	10	11	12
13	14	15	16

Data Out

1	5	9	13
2	6	10	14
3	7	11	15
4	8	12	16

This work borrows ideas from wireless LAN especially the Frame structure that is transmitted into the medium.

Fig. 3: Proposed Frame Format

SYNC (15 ON OFF)	SFD (2 ON OFF)	LENGTH (2SYMBOLS)	CRC (2 symbols)	DATA (2000 BYTES)

_____ON/OFF_____PPM_____

Sync field: It consistas of alternante ones and zeros. One represents pulse ON for a period of 20 ns while the zero represents pulse OFF period of100us.a. This field information is known by the receiver. When the receiver is turned on it first looks for this “1”, “0” repetition in the incoming signal to distinguish the desired signal from thenoise. Start of Frame Delimiter (SFD):a.It consists of a ON-OFF pattern that is dis-similar to the sync repetitionpattern.b.The main purpose of this is to let the receiver, once latched to the sync pattern, to adjust its local clock –frame synchronization. LengthField: a. This field consists of length information encoded by two PPMsymbols. This field is needed by the RX, as it needs to know how many data bytes to expe22ctin thepayload. Cyclic Redundancy Check (CRC) field: a. This field contains the 16 –CRC checksum which is modulated as two PPM symbolsfor error detection over the length field.a. Polynomialused: $z^{16}+ z^{15} + z^{2}+1$Data payload: a. This contains the actual data from the interleaver.b.It is modulated using PPM.

TX Block Diagram

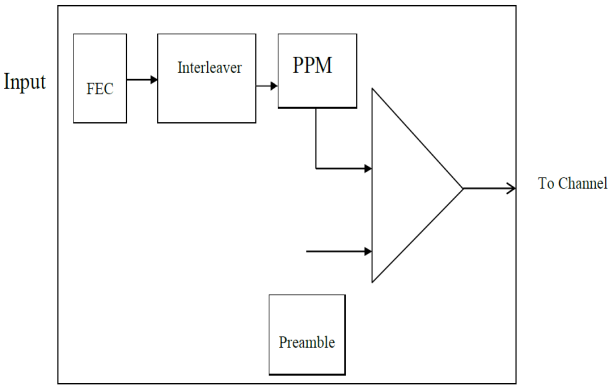

Fig.4: TX Block Diagram

4. Receiver Design

Unlike the TX design, where it began with individuel blocks and finally ended with block diagram (*Botttom –up approach*), the RX design follows a reverse approach, i.e. it starts with the overall block diagram and ends with tweaking the performance of individual blocks (Top – Down approach).

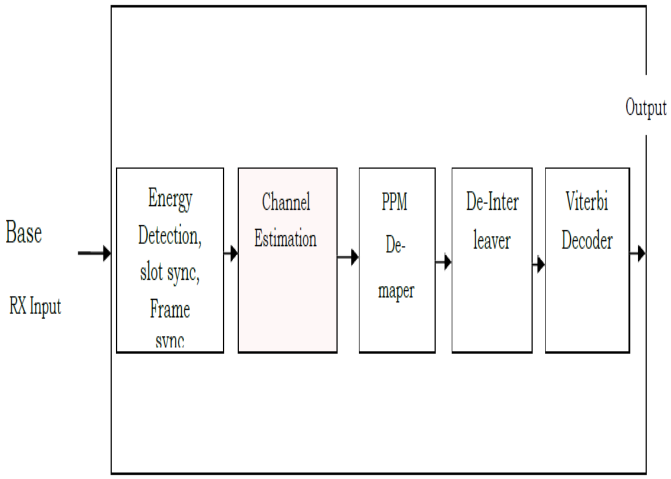

Figure 5: RX Block Diagram

Whenever the RX is turned on, it first calculates noise threshold for a couple of intervals. Once the noise threshold is calculated, it starts looking for the **SYNC** pattern in the incoming signal. Sync pattern, as discussed in previous Sec 3.5, is basically a sequence of alternating pulse ON and OFF repetition pattern.
Once the RX finds the sync pattern, it ***latches*** on to the incoming signal until it encounters **SFD** field. SFD field is a unique pattern that is different from SYNC, so that the receiver when identifies this SFD pattern, knows that SYNC field has completed and after the SFD field it should expect the PPM Modulated datafields.

5. Channel Estimation

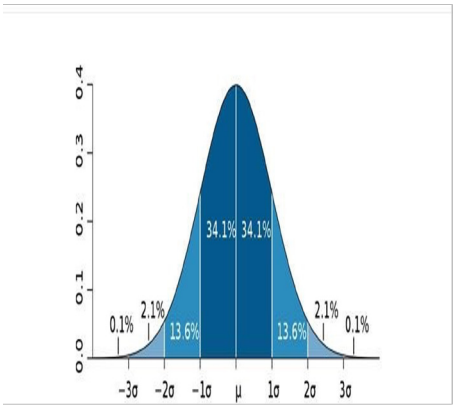

Figure 6: Gaussian Distribution**.**

Because of the FSO channel properties, the signal might undergo dispersion. To overcome that, a channel estimation technique must be used. But the scope of the current work does not include that and the only channel effect that is included in the work is noise.

PPM-Demapper

After the RX has performed frame synchronization through SFD field, it then demodulates

the sub-sequent fields through PPM Demodulation.
The first field it encounters is two PPM symbols containing information of number of bytes in the payload. It then performs the 16 bit CRC on those fields locally and checks the value with the two PPM symbols of CRC field (PPM de-modulated) value that exists after the length field in the RX data.
If the calculate CRC value does not match with the valued present in the received CRC field, then RX decides that the frame is corrupt and is discarded. If not, then it goes ahead decoding the sub-sequent field which contains the actual PPM modulated message.

PPM Demodulation:

PPM demodulation is very simple. It looks for the slot location where the maximum pulse amplitude is detected. If that maximum pulse amplitude is greater than the noise threshold then the slot number, where the maximum is observed is declared as the PPM de-mapped value. It exactly an inverse process of PPMmodulation.

De-Interleaver

Since an interleaver is used at the TX, it is only natural that an inverse operation needs to be performed at the RX. The interleaver used in the TX is a 4x4 Row-in-Column-Out block interleaver. To get the correct order of the data back, a row-in-column-out operation has to be performed at the RX. This turns out to be the same operation the intrleaver performed at the TX. Essentially the same Interleaver resource can be used even for de-interleaver.

Viterbi Decode

A Viterbi Decoder is needed at the RX as a convolutional encoder is used at the TX. The theory of Viterbi decoder is not covered here as it is exhaustively discussed in the literature. Here only the specifications of the decoder are discussed.A hard-decision Viterbi decoder with a trace back length of 8, that matches with the polynomials used in the convolutional encoder is designed. The output of the decoder is the final message bits. From the above discussions, it is clear that the design of the RX is completely driven by the choices made in the TX design.

From the discussion of the earlier chapter, it is clear that the TX signal is mostly *sparse.* ON pulse duration is of only 2 samples, while OFF pulse duration is of approximately 10,000 samples. Hence if we calculate variance at any random time, it gives us a close estimate of the noise power spectral density.

$$= \frac{\sum_{n=0}^{N-1} |r(n)|^2}{N}$$

The value of Nused in the work is 256.

It is a well-known fact that for a Gaussian distribution of mean μ and standard deviation σ, the probability of the sample value exceeding |3 σ| is less than 0.1%, see figure 6.

6. Results and Discussions

Optimum number of bits per PPM symbol

The modulation scheme employed in this design is discussed in Sec 3.2. But it didn't give any explantation on the optimum number of bits to be used per symbol.
Here *Optimum* means achevions high data rate

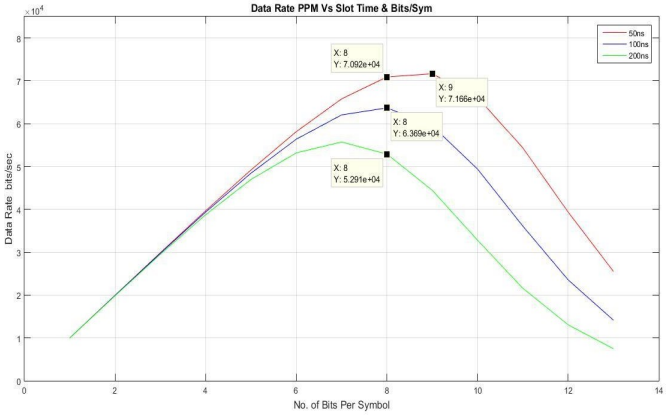

Fig.7: Data Rate Vs. No. of Bits/Symb

From the above figure, the following observations can be made,As overall slot duration decreases, data rate increases and its obvious because the lesser the symbol duration the better the datarate.For a given slot duration, data rate increases as the number of bits per symbol,increasesuntilacertainandthendecreases,becauseinitiallywaitslotisgreaterthantheactual PPM symbol, but as we keep on increasing the number of bits per symbol, the contribution of PPM symbol time to the effective time becomes comparable and it yields diminishingreturns.For a slot duration of 100ns, the maximum data rate of 63.6kbps occurs at 8-bits per symbol which coincidentally matches with the notion of bytes. Hence the choice of 8-bits per symbol and PPM slot duration of 100ns is used in the current design.

Effect of Preamble on Effective DataRate

In the earlier section, the data rate calculation is purely based on the actual payload. But as mentioned in Sec 3.5, there is a frame format and actual data is only one field among many. Hence the effective data calculation should account for the entire preamble overhead. Obviously with 8bits/symb and slot time of 100ns, the effective data rate will be less than the 63.6kbps. In fact it is a function of the number of bytes of the payload.
This analysis is presented in the figure 8 below

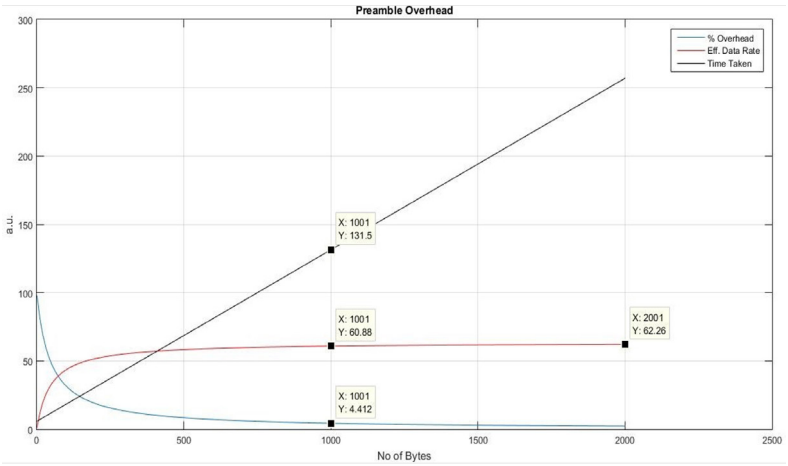

Figure 8: Effect of Preamble Overhead

From the above fig 8, the following observations can be made.The effective data rate (red colour line) increases steadily with the size of payload and it reaches 63kbps asymptotically for bigpayloadsPreamble Overhead percentage (blue line), decreases once again as the payload size increasesFor around 2000 bytes of data, the overall time taken is approximately only 260ms.

6.1. System Performance

In this section, the simulation result of the end-to-end communication link is presented. A BER Vs Es/No analysis is presented in figure 9

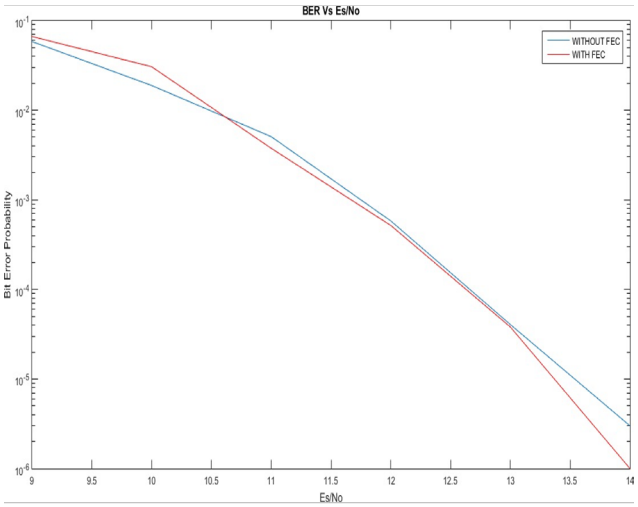

Fig 9: BER Vs Es/No of the PPM Modem

BER of $10^{\wedge -6}$ is achieved at Es/No of above14dB.

Note: Eb/No (dB) = Es/No (dB) - 10log(bits per symbol)

Eb/No (dB) = Es/No (dB) – 9

7. Conclusions

The research work started with a modest of objective designing a FSO communication link that achieves a data rate of more than 20kbps with a BER performance of 10^{-6}. However the laser source with a pulse repetition interval of 100us posed a serious limitation on data rate to 312 bps.

To overcome that limitation, we proposed a modified PPM technique that meets the data rate requirement. The problem of synchronization came as a by-product of the PPM scheme.

To overcome that, we proposed an *extended slot duration* technique that is very simple to implement in hardware when compared to the traditional synchronization techniques. Although the proposed technique slightly deteriorates the data rate, it is right as it meets the project data rate requirements.

An exhaustive mat lab simulation confirmed the proposed design indeed met the project requirements.

As a future work, I intend to port this algorithm on an FPGA and test the performance in the real world.

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